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类脑智能 驱动未来

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SATA 一致性测试原理与方法

BY NeuHelium

类脑智能 驱动未来

目录

- SATA3.0测试简介及N5411B一致性测试软件操作方法
- 手动测试SATA3.0眼图和抖动等参数
- SigTest测试方法
- 电缆校准和De-Skew的方法

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SATA3.0 物理层测试参数

Physical Layer

PHY, TSG, OOB 测试
- 发射端信号质量

PHY-01 : Unit Interval
PHY-02 : Frequency Long Term Stability
PHY-03 : SSC Modulation Frequency
PHY-04 : SSC Modulation Deviation
TSG-01 : Differential Output Voltage
TSG-02 : Rise/Fall Time
TSG-03 : Differential Skew
TSG-04 : AC Common Mode Voltage
TSG-05 : Rise/Fall Imbalance
TSG-06 : Amplitude Imbalance
TSG-09 : Gen1 (1.5Gb/s) TJ
TSG-10 : Gen1 (1.5Gb/s) DJ
TSG-11 : Gen2 (3Gb/s) TJ
TSG-12 : Gen2 (3Gb/s)
TSG-13 : Gen3 (6Gb/s) Transmit Jitter
TSG-14 : Gen3 (6Gb/s) Max Diff Vamp
TSG-15 : Gen3 (6Gb/s) Min Diff Vamp
TSG-16 : Gen3 (6Gb/s) AC Com Mode Voltage

OOB-01 : OOB Signal Detection Threshold
OOB-02 : UI During OOB Signaling
OOB-03 : COMINIT/RESET/WAKE Burst Length
OOB-04 : COMINIT/RESET Transmit Gap Length
OOB-05 : COMWAKE Transmit Gap Length
OOB-06 : COMWAKE Gap Detection Windows
OOB-07 : COMINIT/RESET Gap Detection Windows

Tx, Rx 测试- 阻抗/回波损耗

RX-01 : Pair Differential Impedance
RX-02 : Single-Ended Impedance (Obsolete)
RX-03 : Gen2 Diff Mode Return Loss
RX-04 : Gen2 Common Mode Return Loss
RX-05 : Gen2 impedance Balance
RX-06 : Gen1 Diff Mode Return Loss
RX-07 : Gen3 Diff Mode Return Loss
RX-08 : Gen3 impedance Balance
TX-01 : Pair Differential Impedance
TX-02 : Single-Ended Impedance (Obsolete)
TX-03 : Gen2 Differential Mode Return Loss
TX-04 : Gen2 Common Mode Return Loss
TX-05 : Gen2 Impedance Balance
TX-06 : Gen1 Differential Mode Return Loss
TX-07 : Gen3 Differential Mode Return Loss
TX-08 : Gen3 Impedance Balance

RSG测试
-接收测试

RSG-01 : Gen1 (1.5Gb/s) Receiver Jitter Test
RSG-02 : Gen2 (3Gb/s) Receiver Jitter Test
RSG-03 : Gen3 (6Gb/s) Receiver Jitter Test
RSG-05 : Receiver stress Test at +350ppm (Informative)
RSG-06 : Receiver stress Test with SSC (Informative)

SATA 3.0 简介及测试方案

SATA 3.0 技术简介

SATA 3.0的信号速率为6Gbps，向下兼容2.0和1.0规范的要求。规范对发射端的测试规定示波器带宽至少为 12GHz或者更高，3.0规范增加了对AC共模噪声的测试要求、以及经CIC(一致性互联通道)前后抖动的测试，这要求在测试仪器能够保证最佳的本底噪性能，以及仪器能够提供规范要求的抖动传递函数。

SATA 3.0 发射端测试规范内容

PHY, TSG, OOB

SATA 3.0 发射端测试方案

- 测试仪器

  DSA91204A或者DSA-X90000A系列示波器
  81134A（测试OOB）

- 测试软件

  一致型测试软件N5411B或SigTest软件

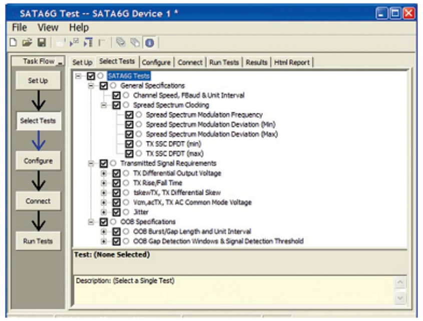
  协议解码分析软件N8801A

- 测试夹具及附件

  15443A SMA 等长电缆

  11742A 隔直器

  TF-SATA-NE-ZP 或其他测试夹具


SATA6G Test -- SATA6G Device 1 *
File
View
Help
Task Flow
Set Up
Select Tests
Configure
Connect
Run Tests
Results
Html Report

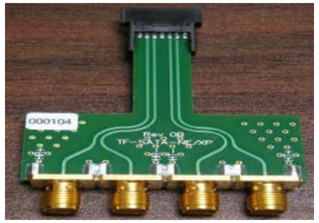
- ☑ ○ SATA6G Tests
  - ☑ ○ General Specifications
    - ☑ ○ Channel Speed, FBaud & Unit Interval
    - ☑ ○ Spread Spectrum Clocking
      - ☑ ○ Spread Spectrum Modulation Frequency
      - ☑ ○ Spread Spectrum Modulation Deviation (Min)
      - ☑ ○ Spread Spectrum Modulation Deviation (Max)
      - ☑ ○ TX SSC DFDT (min)
      - ☑ ○ TX SSC DFDT (max)
  - ☑ ○ Transmitted Signal Requirements
    - ☑ ○ TX Differential Output Voltage
    - ☑ ○ TX Rise/Fall Time
    - ☑ ○ tskewTX, TX Differential Skew
    - ☑ ○ Vcm,acTX, TX AC Common Mode Voltage
    - ☑ ○ Jitter
  - ☑ ○ OOB Specifications
    - ☑ ○ OOB Burst/Gap Length and Unit Interval
    - ☑ ○ OOB Gap Detection Windows & Signal Detection Threshold

Test: (None Selected)

Description: (Select a Single Test)

SATA 6G Test Report

Overall Results: 1 of 14 Tests Failed



Summary of Results

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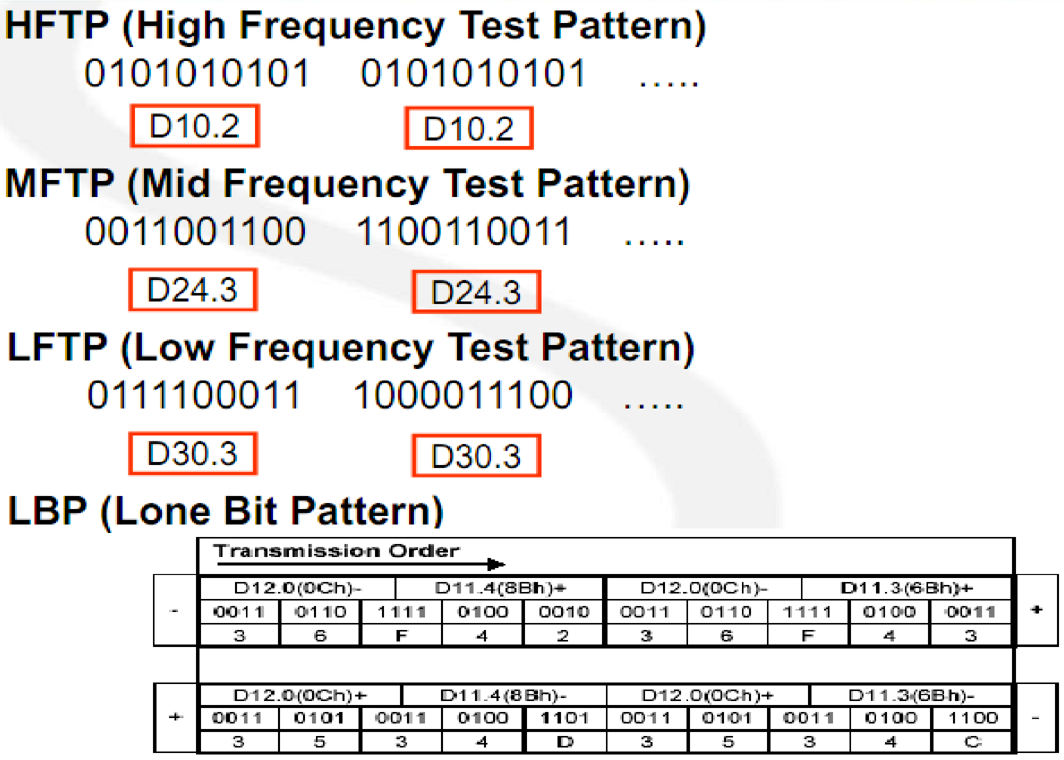
规范里定义的测试码型

- SATA规范里定义了一些pattern用以测试测试规范要求的测试内容需要配置芯片到BIST-L模式，使用81134A和N4903B发出测试码型让DUT环回生成测试码型。或者芯片可以直接配置输出这些pattern。
- 一致性测试软件里会根据选择的不同测量项目，提示切换测试码型，在切换完成后再继续软件的执行。



HFTP (High Frequency Test Pattern)

0101010101 0101010101 …..

D10.2 D10.2

MFTP (Mid Frequency Test Pattern)

0011001100 1100110011 …..

D24.3 D24.3

LFTP (Low Frequency Test Pattern)

0111100011 1000011100 …..

D30.3 D30.3

LBP (Lone Bit Pattern)

Transmission Order

	D12.0(0Ch)-		D11.4(8Bh)+			D12.0(0Ch)-		D11.3(6Bh)+			
-	0011	0110	1111	0100	0010	0011	0110	1111	0100	0011	+
	3	6	F	4	2	3	6	F	4	3	

	D12.0(0Ch)+		D11.4(8Bh)-			D12.0(0Ch)+		D11.3(6Bh)-			
+	0011	0101	0011	0100	1101	0011	0101	0011	0100	1100	-
	3	5	3	4	D	3	5	3	4	C	

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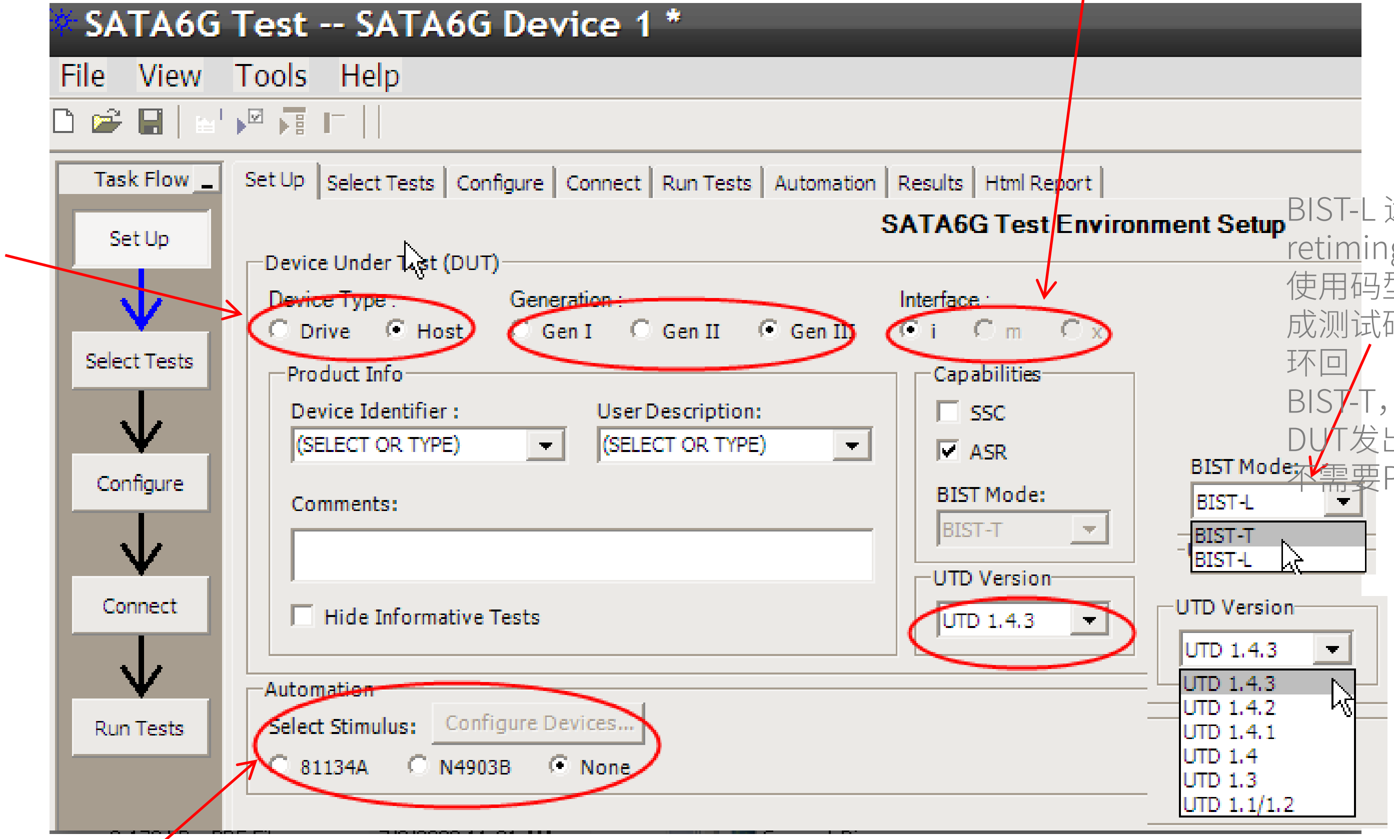
N5411B软件的设置

i: 内部接口，PC主板和硬盘直接相连
m: 短背板和外部连接
x: 长背板和系统到系统应用

DUT类型


SATA6G Test -- SATA6G Device 1 *
File
View
Tools
Help
Task Flow
Set Up
Select Tests
Configure
Connect
Run Tests
Set Up
Select Tests
Configure
Connect
Run Tests
Automation
Results
Html Report

SATA6G Test Environment Setup

Device Under Test (DUT)

Device Type : ○ Drive ● Host

Generation : ○ Gen I ○ Gen II ● Gen III

Interface : ● i ○ m ○ x

Product Info

Device Identifier : (SELECT OR TYPE)

User Description: (SELECT OR TYPE)

Comments:

☐ Hide Informative Tests

Capabilities

☐ SSC

☑ ASR

BIST Mode: BIST-T

UTD Version: UTD 1.4.3

Automation

Select Stimulus: Configure Devices...

○ 81134A ○ N4903B ● None

BIST Mode: BIST-L

BIST-T
BIST-L

UTD Version: UTD 1.4.3

UTD 1.4.3
UTD 1.4.2
UTD 1.4.1
UTD 1.4
UTD 1.3
UTD 1.1/1.2

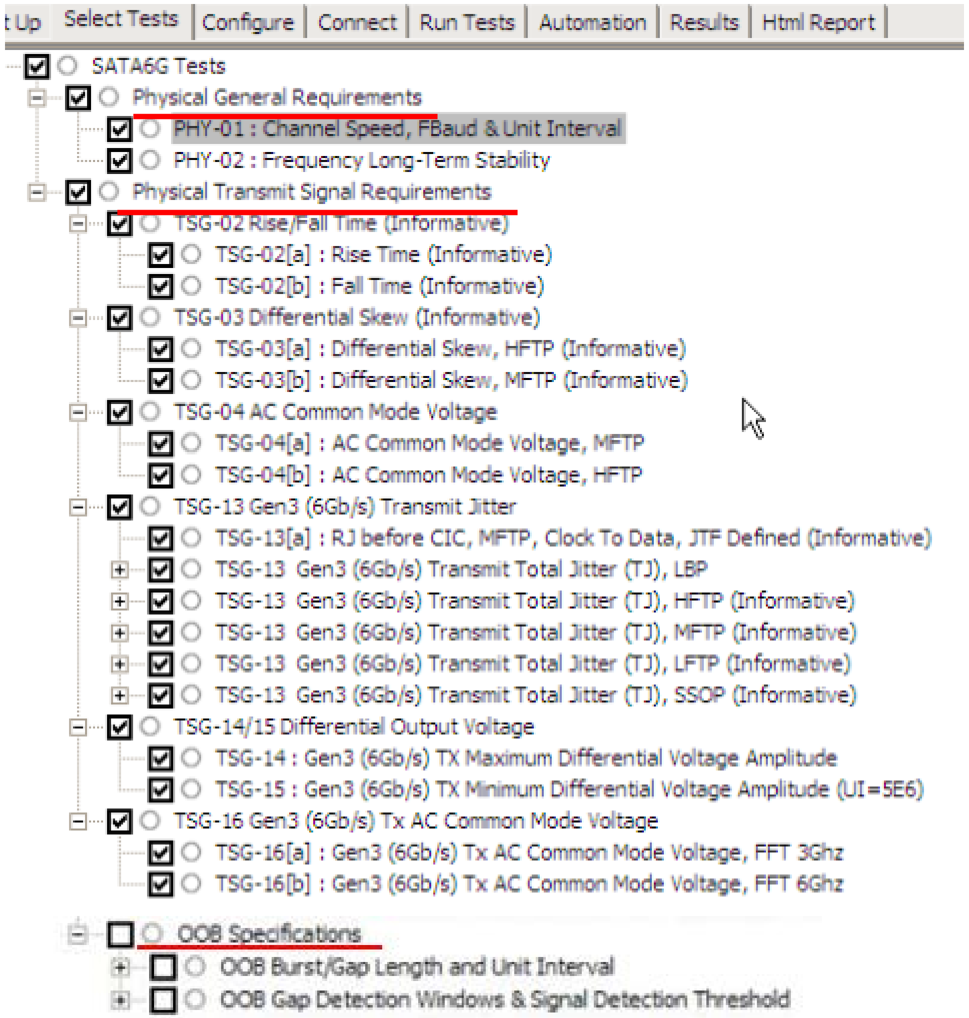
BIST-L 远端retiming环回模式，使用码型发生器生成测试码型，DUT环回
BIST-T，通过配置DUT发出测试码型，不需要PG

United Test Description测试标准

把DUT设置进入BIST-L模式，使用81134A或N4903B生成码型到DUT环回发出测试码型，或用来测试OOB信号

选择测试项

包括PHY , TSG and OOB.



- ☑ ○ SATA6G Tests
  - ☑ ○ Physical General Requirements
    - ☑ ○ PHY-01 : Channel Speed, FBaud & Unit Interval
    - ☑ ○ PHY-02 : Frequency Long-Term Stability
  - ☑ ○ Physical Transmit Signal Requirements
    - ☑ ○ TSG-02 Rise/Fall Time (Informative)
      - ☑ ○ TSG-02[a] : Rise Time (Informative)
      - ☑ ○ TSG-02[b] : Fall Time (Informative)
    - ☑ ○ TSG-03 Differential Skew (Informative)
      - ☑ ○ TSG-03[a] : Differential Skew, HFTP (Informative)
      - ☑ ○ TSG-03[b] : Differential Skew, MFTP (Informative)
    - ☑ ○ TSG-04 AC Common Mode Voltage
      - ☑ ○ TSG-04[a] : AC Common Mode Voltage, MFTP
      - ☑ ○ TSG-04[b] : AC Common Mode Voltage, HFTP
    - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Jitter
      - ☑ ○ TSG-13[a] : RJ before CIC, MFTP, Clock To Data, JTF Defined (Informative)
      - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Total Jitter (TJ), LBP
      - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Total Jitter (TJ), HFTP (Informative)
      - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Total Jitter (TJ), MFTP (Informative)
      - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Total Jitter (TJ), LFTP (Informative)
      - ☑ ○ TSG-13 Gen3 (6Gb/s) Transmit Total Jitter (TJ), SSOP (Informative)
    - ☑ ○ TSG-14/15 Differential Output Voltage
      - ☑ ○ TSG-14 : Gen3 (6Gb/s) TX Maximum Differential Voltage Amplitude
      - ☑ ○ TSG-15 : Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude (UI=5E6)
    - ☑ ○ TSG-16 Gen3 (6Gb/s) Tx AC Common Mode Voltage
      - ☑ ○ TSG-16[a] : Gen3 (6Gb/s) Tx AC Common Mode Voltage, FFT 3Ghz
      - ☑ ○ TSG-16[b] : Gen3 (6Gb/s) Tx AC Common Mode Voltage, FFT 6Ghz
  - ☐ ○ OOB Specifications
    - ☐ ○ OOB Burst/Gap Length and Unit Interval
    - ☐ ○ OOB Gap Detection Windows & Signal Detection Threshold

PHY

TSG

OOB

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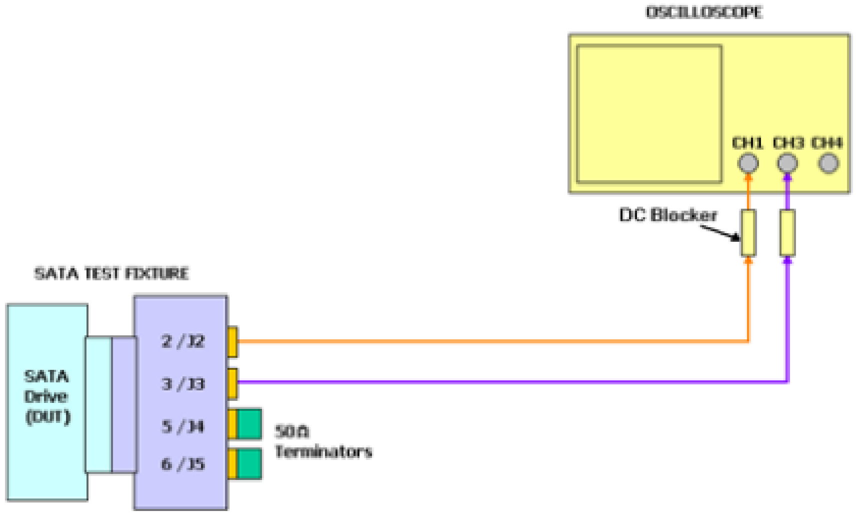
连接指南

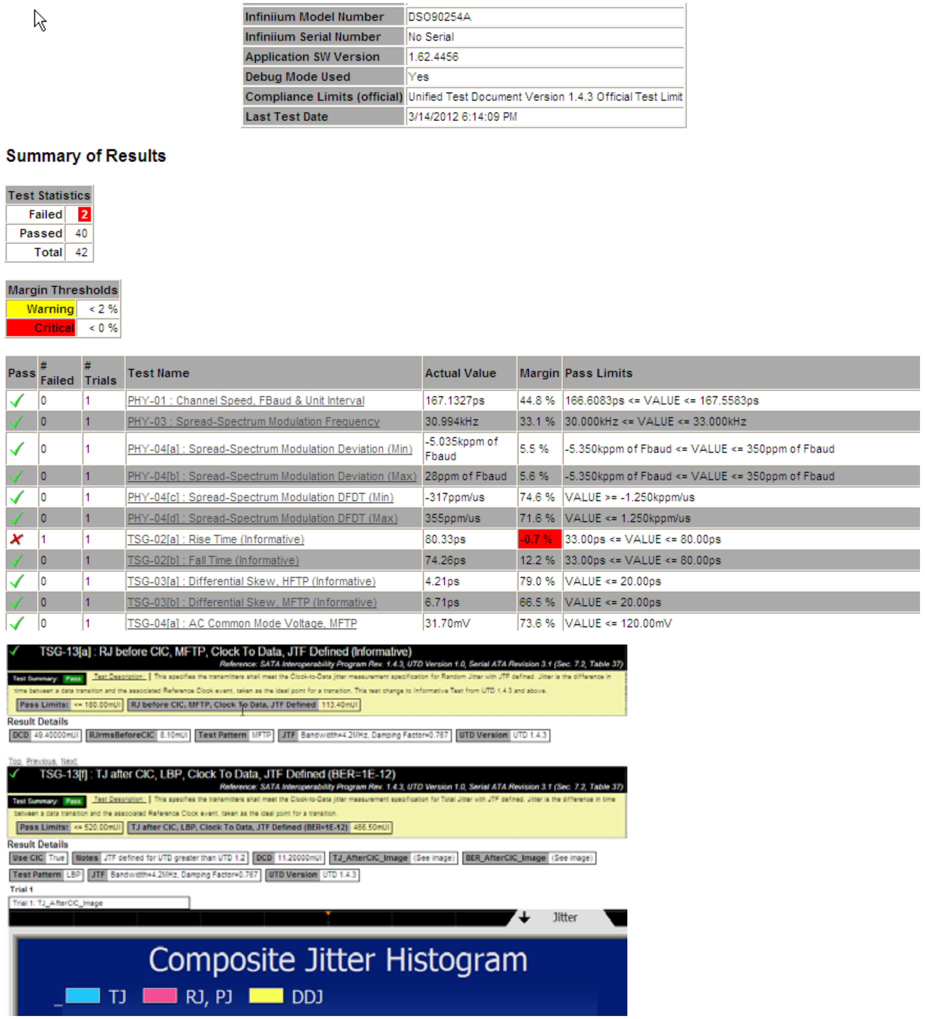
根据连接示意图连接仪器，通过夹具和SMA电缆(需要De-Skew)连接到示波器的1/3通道，推荐使用DC Block，注意如果使用81134A或N4903B的连接方式有所差别


OSCILLOSCOPE
CH1
CH3
CH4
DC Blocker
SATA TEST FIXTURE
SATA Drive (DUT)
2 /J2
3 /J3
5 /J4
6 /J5
50Ω Terminators

Connect a 50 Ω SMA terminator to **6 (J5)** of the test fixture.
Connect a 50 Ω SMA terminator to **5 (J4)** of the test fixture.
Connect the SMA Cable from **3 (J3)** of the test fixture to **CH3** of the oscilloscope via a **11742A** DC blocker.
Connect the SMA Cable from **2 (J2)** of the test fixture to **CH1** of the oscilloscope via a **11742A** DC blocker.
NOTE: Please ensure that the SMA cables deskew calibration has been performed prior to running the test(s)

测试结果与报告

生成测试报告后，File---Save Project As，指定目录后即可保存报告和相关的问题，在对应目录内的report.html文件就是报告文件



Infiniium Model Number	DSO90254A
Infiniium Serial Number	No Serial
Application SW Version	1.62.4456
Debug Mode Used	Yes
Compliance Limits (official)	Unified Test Document Version 1.4.3 Official Test Limit
Last Test Date	3/14/2012 6:14:09 PM

Summary of Results

Test Statistics	
Failed	2
Passed	40
Total	42

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	PHY-01 : Channel Speed, FBaud & Unit Interval	167.1327ps	44.8 %	166.6083ps <= VALUE <= 167.5583ps
✓	0	1	PHY-03 : Spread-Spectrum Modulation Frequency	30.994kHz	33.1 %	30.000kHz <= VALUE <= 33.000kHz
✓	0	1	PHY-04[a] : Spread-Spectrum Modulation Deviation (Min)	-5.035kppm of Fbaud	5.5 %	-5.350kppm of Fbaud <= VALUE <= 350ppm of Fbaud
✓	0	1	PHY-04[b] : Spread-Spectrum Modulation Deviation (Max)	28ppm of Fbaud	5.6 %	-5.350kppm of Fbaud <= VALUE <= 350ppm of Fbaud
✓	0	1	PHY-04[c] : Spread-Spectrum Modulation DFDT (Min)	-317ppm/us	74.6 %	VALUE >= -1.250kppm/us
✓	0	1	PHY-04[d] : Spread-Spectrum Modulation DFDT (Max)	355ppm/us	71.6 %	VALUE <= 1.250kppm/us
✗	1	1	TSG-02[a] : Rise Time (Informative)	80.33ps	-0.7 %	33.00ps <= VALUE <= 80.00ps
✓	0	1	TSG-02[b] : Fall Time (Informative)	74.26ps	12.2 %	33.00ps <= VALUE <= 80.00ps
✓	0	1	TSG-03[a] : Differential Skew, HFTP (Informative)	4.21ps	79.0 %	VALUE <= 20.00ps
✓	0	1	TSG-03[b] : Differential Skew, MFTP (Informative)	6.71ps	66.5 %	VALUE <= 20.00ps
✓	0	1	TSG-04[a] : AC Common Mode Voltage, MFTP	31.70mV	73.6 %	VALUE <= 120.00mV

✓ TSG-13[a] : RJ before CIC, MFTP, Clock To Data, JTF Defined (Informative)

Reference: SATA Interoperability Program Rev. 1.4.3, UTD Version 1.0, Serial ATA Revision 3.1 (Sec. 7.2, Table 37)

Test Summary: Pass | Test Description: | This specifies the transmitters shall meet the Clock-to-Data jitter measurement specification for Random Jitter with JTF defined. Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition. This test change to Informative Test from UTD 1.4.3 and above.

Pass Limits: <= 180.00mUI | RJ before CIC, MFTP, Clock To Data, JTF Defined 113.40mUI

Result Details

DCD 49.40000mUI | RJrmsBeforeCIC 8.10mUI | Test Pattern MFTP | JTF Bandwidth=4.2MHz, Damping Factor=0.767 | UTD Version UTD 1.4.3

Top, Previous, Next

✓ TSG-13[f] : TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12)

Reference: SATA Interoperability Program Rev. 1.4.3, UTD Version 1.0, Serial ATA Revision 3.1 (Sec. 7.2, Table 37)

Test Summary: Pass | Test Description: | This specifies the transmitters shall meet the Clock-to-Data jitter measurement specification for Total Jitter with JTF defined. Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition.

Pass Limits: <= 520.00mUI | TJ after CIC, LBP, Clock To Data, JTF Defined (BER=1E-12) 466.50mUI

Result Details

Use CIC True | Notes JTF defined for UTD greater than UTD 1.2 | DCD 11.20000mUI | TJ_AfterCIC_Image (See image) | BER_AfterCIC_Image (See image)

Test Pattern LBP | JTF Bandwidth=4.2MHz, Damping Factor=0.767 | UTD Version UTD 1.4.3

Trial 1

Trial 1: TJ_AfterCIC_Image

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- SigTest测试方法
- 电缆校准和De-Skew的方法

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手动测试SATA说明

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- 本部分主要用于DUT无法发出标准要求的HFTP / MFTP / LFTP / LBP等码型，另外需要测试眼图模板的要求等，需要采用眼图测试的方式得到以下几项测试结果

1. 测试模板
2. 手动测试眼图
3. TX输出信号幅度
4. 测试上升/下降时间

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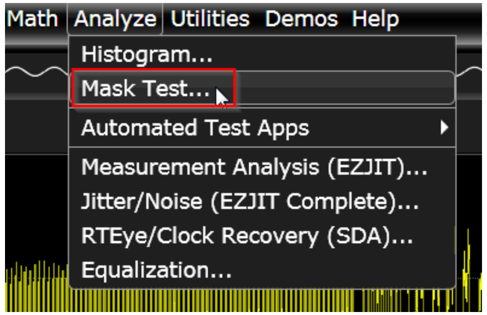
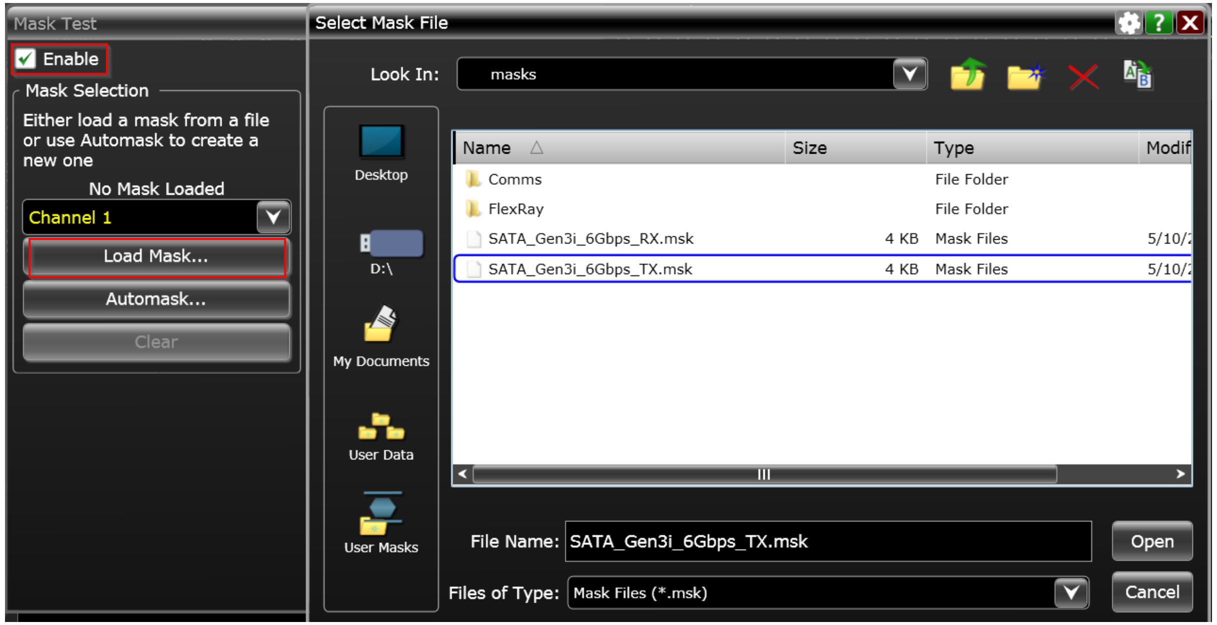
SATA 模板测试

SATA 规范并没有模板测试的要求，实际上规范通过对抖动Tj和幅度上的测量来体现对信号的要求，下面是模板测试步骤。

- 首先接上夹具电缆和示波器，DUT上电会设置输出Align信号
- 先把1/3通道连接上信号，调整垂直灵敏度，使得1/3通道信号都能够满屏显示，然后点Setup---Channel 1---勾选Differential Channel 1&3，然后把3通道关闭，
- 点击Analyze----Mask Test----点Load Mask(左下角Mask Test Source选择ch1-ch3)… 模板选择对应速率的Tx的模板


Math
Analyze
Utilities
Demos
Help
Histogram...
Mask Test...
Automated Test Apps
Measurement Analysis (EZJIT)...
Jitter/Noise (EZJIT Complete)...
RTEye/Clock Recovery (SDA)...
Equalization...


Mask Test
Select Mask File
Desktop
D:\
My Documents
User Data
User Masks
Open
Cancel
Load Mask...
Automask...
Clear

☑ Enable

Mask Selection

Either load a mask from a file or use Automask to create a new one

No Mask Loaded

Channel 1

Look In: masks

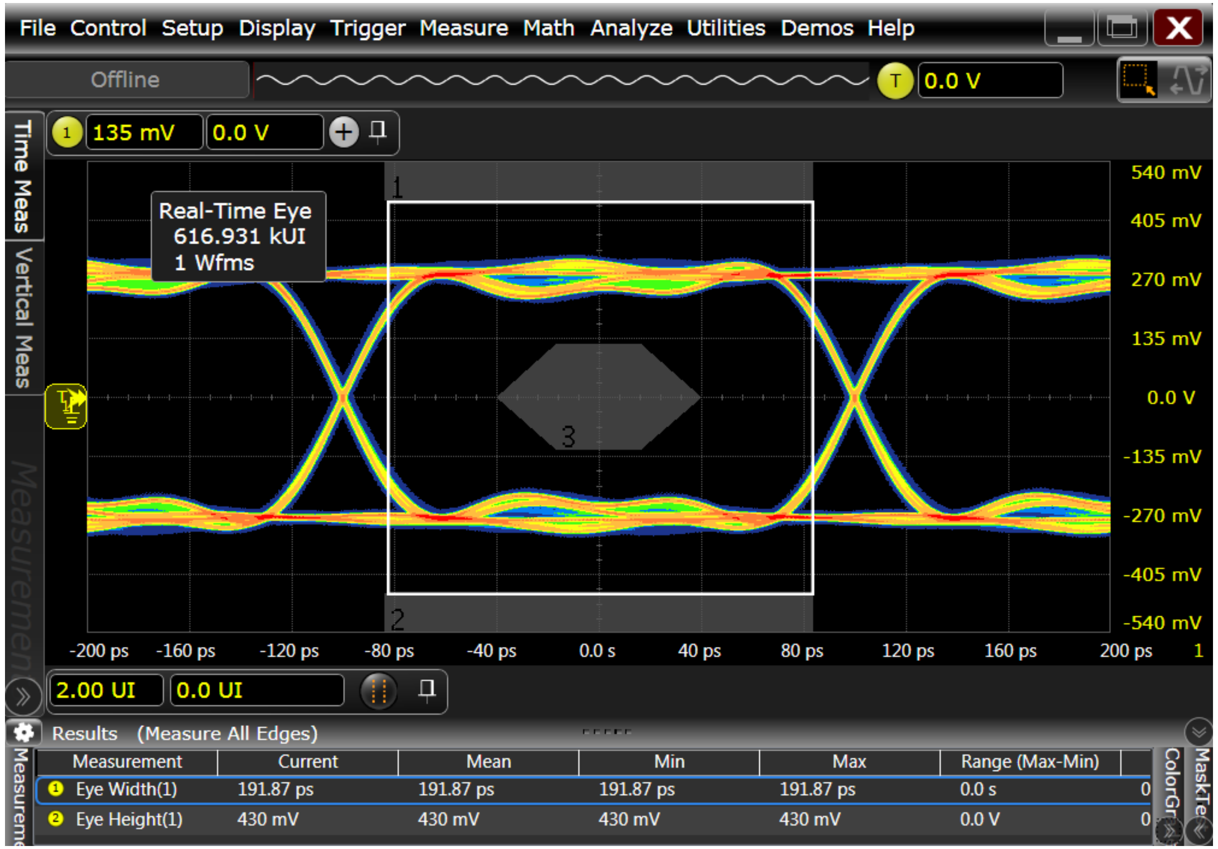
Name	Size	Type	Modif
Comms		File Folder	
FlexRay		File Folder	
SATA_Gen3i_6Gbps_RX.msk	4 KB	Mask Files	5/10/
SATA_Gen3i_6Gbps_TX.msk	4 KB	Mask Files	5/10/

File Name: SATA_Gen3i_6Gbps_TX.msk

Files of Type: Mask Files (*.msk)

测量眼高/眼宽/眼抖动/上升下降时间

- 测量眼图参数，选择菜单Measure→Eye Pattern→Eye Height, Eye Width, Eye Jitter
- 点Measure---Time---Rise/Fall Time(注意在测量上升/下降时间之前先在Measure----Thresholds----选择20%,80% threshold)
- 在波形下方就会显示出测量结果


File Control Setup Display Trigger Measure Math Analyze Utilities Demos Help
Offline
T 0.0 V
1 135 mV 0.0 V
Time Meas
Vertical Meas
Measurements
540 mV
405 mV
270 mV
135 mV
0.0 V
-135 mV
-270 mV
-405 mV
-540 mV
1
2
3
-200 ps
-160 ps
-120 ps
-80 ps
-40 ps
0.0 s
40 ps
80 ps
120 ps
160 ps
200 ps
2.00 UI
0.0 UI
ColorGr
MaskTe

Real-Time Eye
616.931 kUI
1 Wfms

Results (Measure All Edges)

Measurement	Current	Mean	Min	Max	Range (Max-Min)
❶ Eye Width(1)	191.87 ps	191.87 ps	191.87 ps	191.87 ps	0.0 s
❷ Eye Height(1)	430 mV	430 mV	430 mV	430 mV	0.0 V

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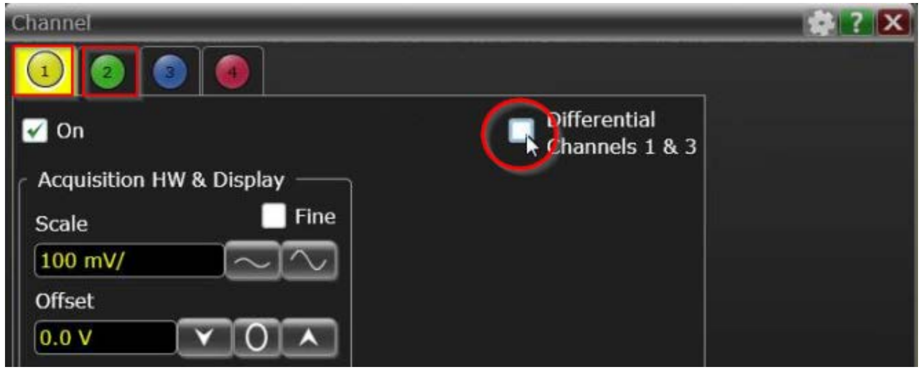
NeuHelium 新氦类脑智能

BY NeuHelium

SATA Sigtest测试示波器设置

1. 通道设置

- 示波器1，3通道通过SMA电缆连接好夹具和被测件
- 调整1/3通道的垂直刻度，使得1/3通道信号满屏
- 点Channel 1，选中Differential Channel 1 & Channel 3， 然后把3通 道关闭


Channel
1
2
3
4
Acquisition HW & Display
Fine
Offset

☑ On

☐ Differential Channels 1 & 3

Scale 100 mV/

Offset 0.0 V

SATA Sigtest测试示波器设置续

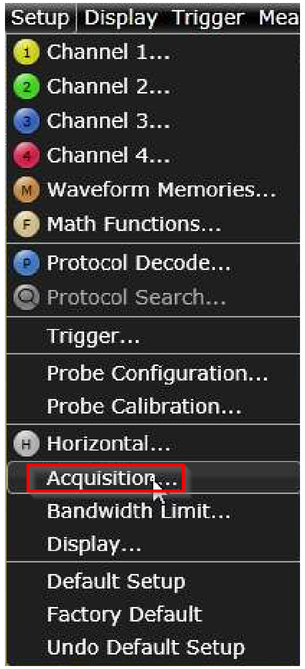
2. 采样设置

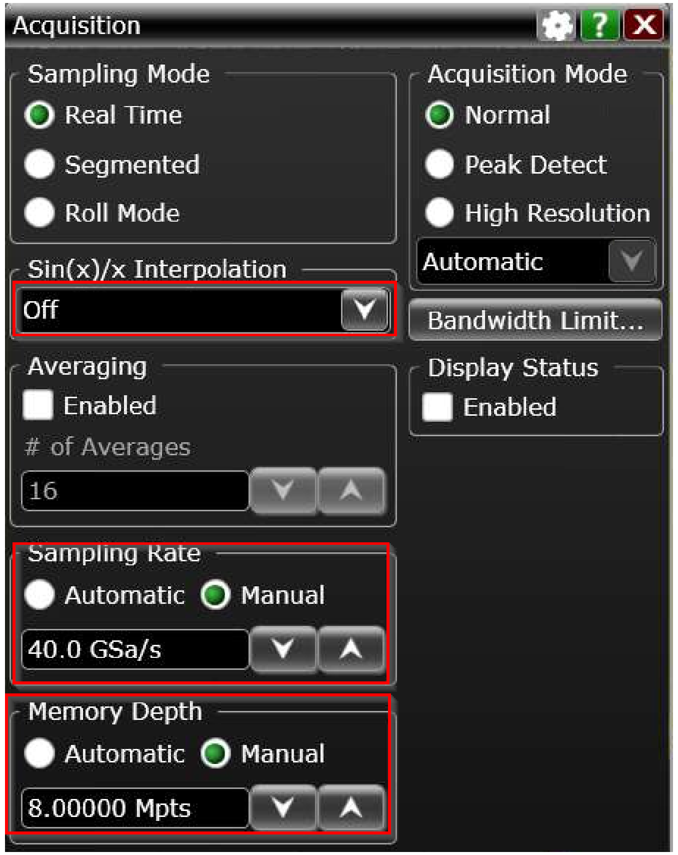
示波器 Setup > Acquisition Sample Rate选择Manual,设置为40GSa/s(Gen1/2可以使用20GSa/s),Memory Depth 设置为10Mpts

注: 因为Intel推荐测试1M个UI，采样深度由采样率和UI数共同决定

Memory Depth = Sample Rate x 1M / (Signal Rate)

Sin(x)/x Interpolation设置为OFF


Setup
Display
Trigger
Mea
Channel 1...
Channel 2...
Channel 3...
Channel 4...
Waveform Memories...
Math Functions...
Protocol Decode...
Protocol Search...
Trigger...
Probe Configuration...
Probe Calibration...
Horizontal...
Acquisition...
Bandwidth Limit...
Display...
Default Setup
Factory Default
Undo Default Setup


Acquisition

Sampling Mode
● Real Time
○ Segmented
○ Roll Mode

Acquisition Mode
● Normal
○ Peak Detect
○ High Resolution
Automatic

Sin(x)/x Interpolation
Off

Averaging
☐ Enabled
# of Averages
16

Display Status
☐ Enabled

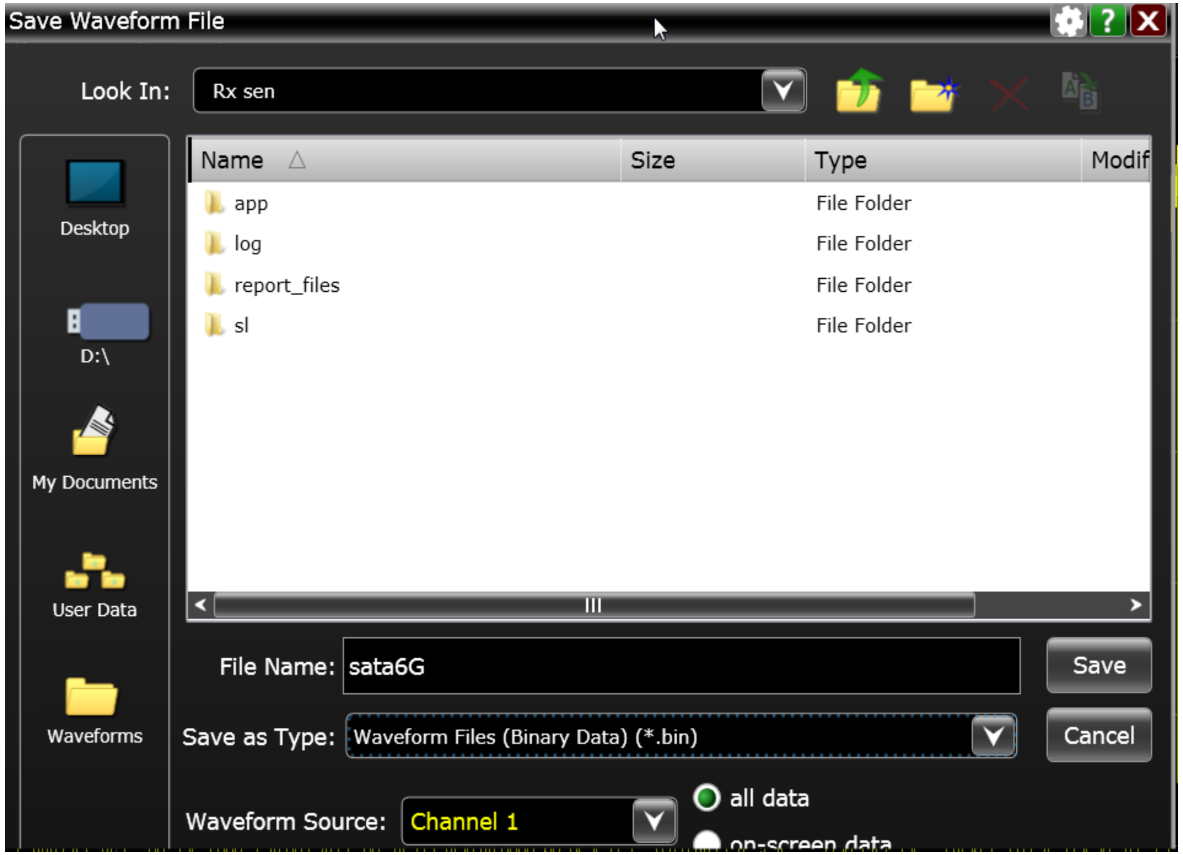
Sampling Rate
○ Automatic ● Manual
40.0 GSa/s

Memory Depth
○ Automatic ● Manual
8.00000 Mpts
Bandwidth Limit...

SATA Sigtest测试示波器设置续

3. 波形保存

- 垂直按触发电平调整按钮或者调整触发电平在0电平
- 按示波器的Run/Stop按钮，或者按下Single按钮
- Save > Waveform， 选择文件类型为Binary Data Files(*.bin)格，Source选择Channel 1 – 3，勾选All Data， 点Save



Save Waveform File

Look In: Rx sen

Name	Size	Type
app		File Folder
log		File Folder
report_files		File Folder
sl		File Folder

File Name: sata6G

Save as Type: Waveform Files (Binary Data) (*.bin)

Waveform Source: Channel 1

● all data

○ on-screen data

Modif
Desktop
D:\
My Documents
User Data
Waveforms
Save
Cancel

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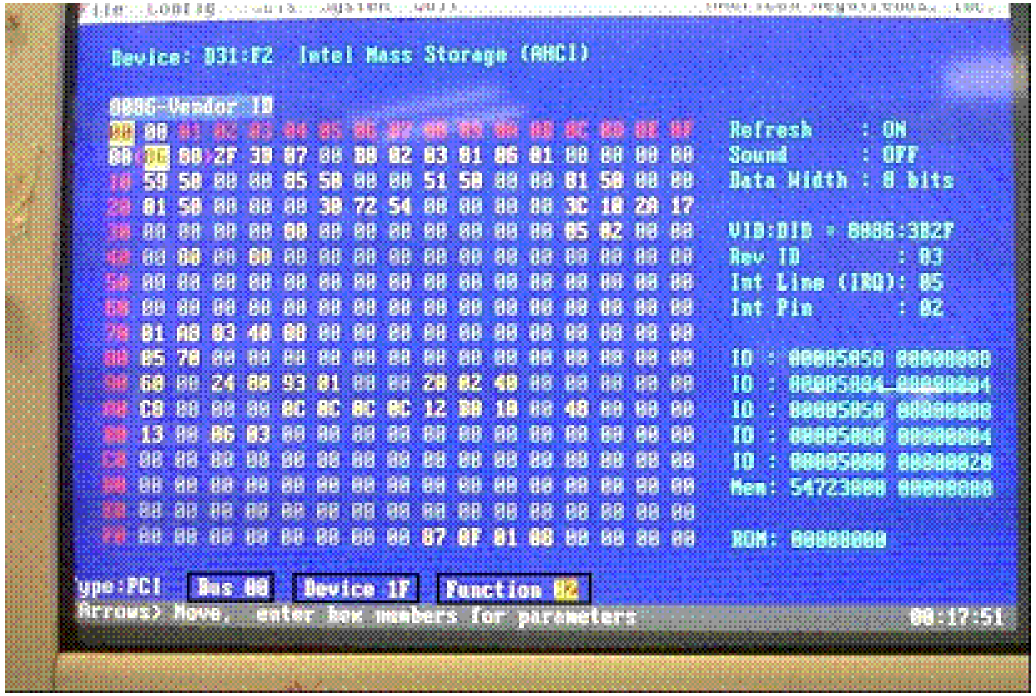
DUT的设置

DUT的设置，需要客户运行RU软件按照Intel或AMD推荐的地址和方法进行设置，具体的设置方法不在本文讨论的范畴

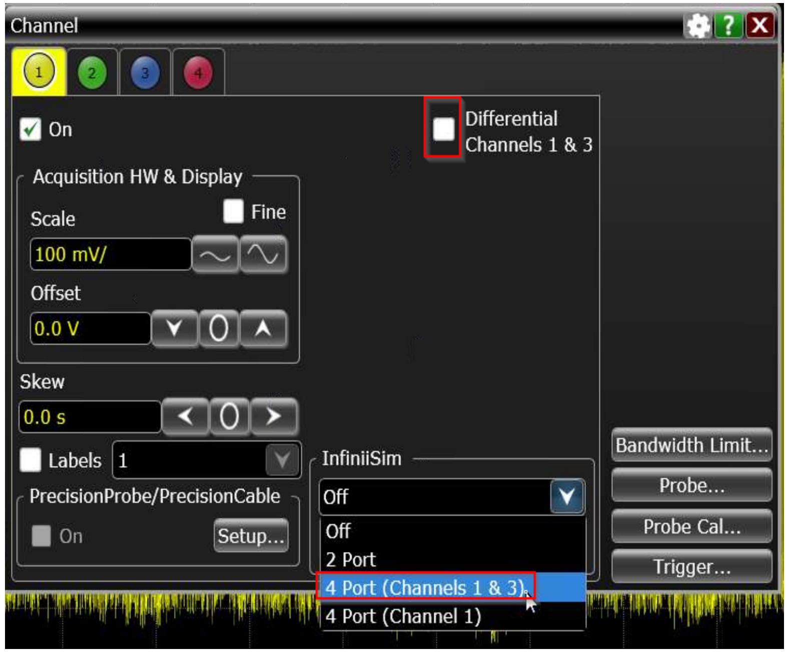


```
Device: D31:F2  Intel Mass Storage (AHCI)

8086-Vendor ID
   86 80 2F 3B 07 00 B0 02 03 01 06 01 00 00 00 00   Sound       : OFF
   59 50 00 00 85 50 00 00 51 50 00 00 81 50 00 00   Data Width : 8 bits
   01 50 00 00 00 30 72 54 00 00 00 00 3C 10 2A 17
   00 00 00 00 80 00 00 00 00 00 00 00 05 02 00 00   VID:DID = 8086:3B2F
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   Rev ID          : 03
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   Int Line (IRQ): 05
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   Int Pin         : 02
   01 A8 03 40 08 00 00 00 00 00 00 00 00 00 00 00
   05 70 00 00 00 00 00 00 00 00 00 00 00 00 00 00   IO : 00005058 00000008
   60 00 24 00 93 01 00 00 20 02 40 00 00 00 00 00   IO : 00005084 00000004
   C0 00 00 00 0C 0C 0C 0C 12 B0 18 00 48 00 00 00   IO : 00005050 00000008
   13 00 06 03 00 00 00 00 00 00 00 00 00 00 00 00   IO : 00005080 00000004
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   IO : 00005000 00000020
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   Mem: 54723000 00000800
   00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
   00 00 00 00 00 00 00 00 87 0F 01 00 00 00 00 00   ROM: 00000000

ype:PCI   Bus 00   Device 1F   Function 02
Arrows> Move,  enter box numbers for parameters                     00:17:51
```

Refresh   : ON

SATA6G测试的特殊要求

Intel规范要求SATA 6G的测试要加入CIC通道以后再用SigTest测试，可以通过示波器软件的InfiniiSim功能嵌入CIC的传递函数模型进行测试，具体方法如下


Channel
1
2
3
4
☑ On
☐ Differential Channels 1 & 3
Acquisition HW & Display
☐ Fine
PrecisionProbe/PrecisionCable
☐ On
Setup...
InfiniiSim
Off
2 Port
4 Port (Channels 1 & 3)
4 Port (Channel 1)
Bandwidth Limit...
Probe...
Probe Cal...
Trigger...

Scale 100 mV/

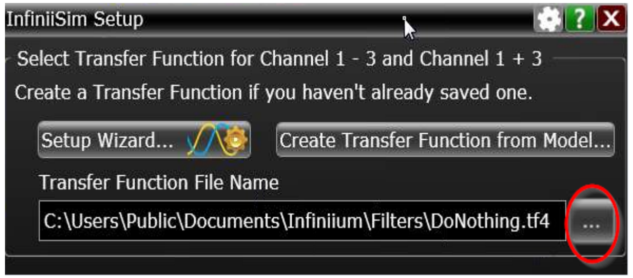
Offset 0.0 V

Skew 0.0 s

☐ Labels 1

InfiniiSim Off

打开InfiniiSim后，选择Bandwidth Limit，设置为13GHz


InfiniiSim Setup
Setup Wizard...
Create Transfer Function from Model...
...

Select Transfer Function for Channel 1 - 3 and Channel 1 + 3

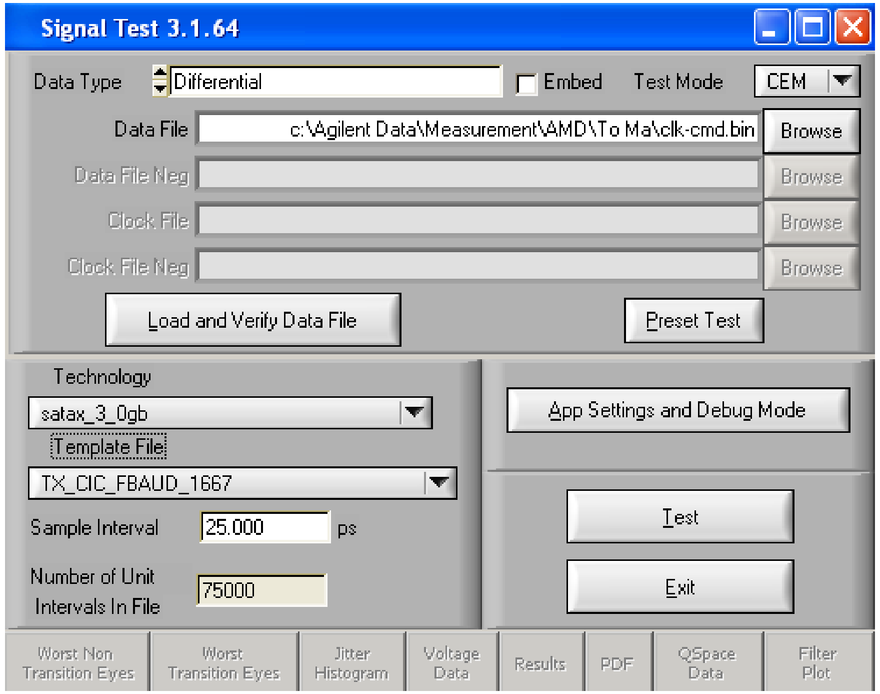
Create a Transfer Function if you haven't already saved one.

Transfer Function File Name C:\Users\Public\Documents\Infiniium\Filters\DoNothing.tf4

选择文件SATA_CIC_4PORT.tf4

SigTest

- 运行SigTest选择保存的*.Bin文件，
- 点Load and Verify Data,
- Technology选择对应的速率等级
- 选择对应的模板Template
- 点击Test



Signal Test 3.1.64

Data Type: Differential

☐ Embed

Test Mode: CEM

Data File: c:\Agilent Data\Measurement\AMD\To Ma\clk-cmd.bin

Data File Neg:

Clock File:

Clock File Neg:

Technology: satax_3_0gb

Template File: TX_CIC_FBAUD_1667

Sample Interval: 25.000 ps

Number of Unit Intervals In File: 75000

Browse
Browse
Browse
Browse
Load and Verify Data File
Preset Test
App Settings and Debug Mode
Test
Exit
Worst Non Transition Eyes
Worst Transition Eyes
Jitter Histogram
Voltage Data
Results
PDF
QSpace Data
Filter Plot

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驱动未来

目录

- SATA3.0测试简介及N5411B一致性测试软件操作方法
- 手动测试SATA3.0眼图和抖动等参数
- SigTest测试方法
- 电缆校准和De-Skew的方法

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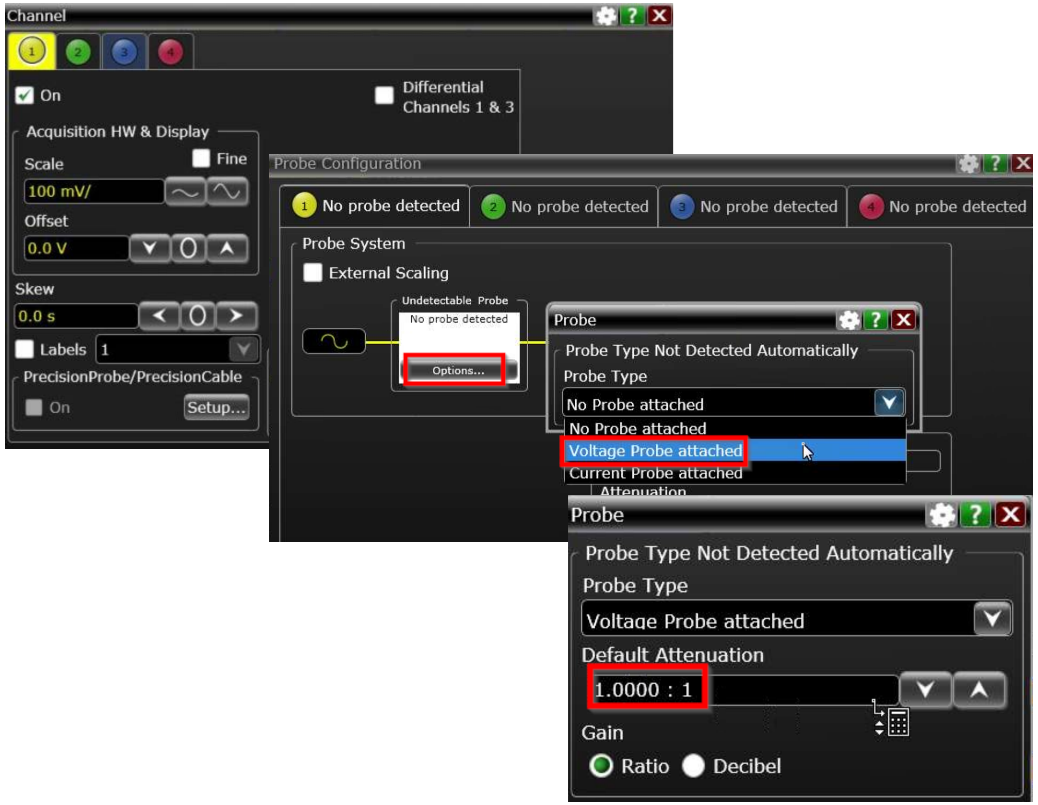
电缆校准

先将Aux Out, Cal Out(DSAX90000A)连接到ch1

Setup---Channel1---Probe Setup，按下面图设置

自定义探头，设置比例1:1，开始校准



Channel

☑ On

☐ Differential Channels 1 & 3

Acquisition HW & Display

Scale: 100 mV/ ☐ Fine

Offset: 0.0 V

Skew: 0.0 s

☐ Labels: 1

PrecisionProbe/PrecisionCable: ☐ On Setup...

Probe Configuration

1 No probe detected | 2 No probe detected | 3 No probe detected | 4 No probe detected

Probe System

☐ External Scaling

Undetectable Probe: No probe detected, Options...

Probe

Probe Type Not Detected Automatically

Probe Type: No Probe attached

No Probe attached

Voltage Probe attached

Current Probe attached

Attenuation

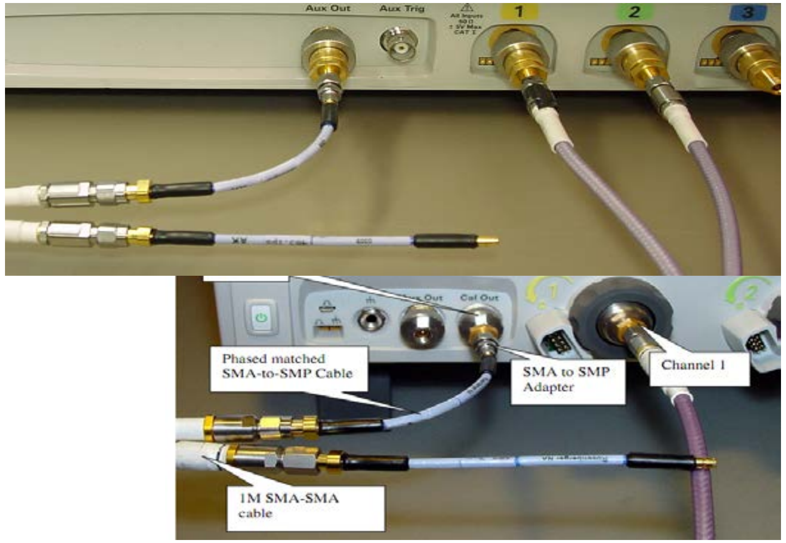
Probe

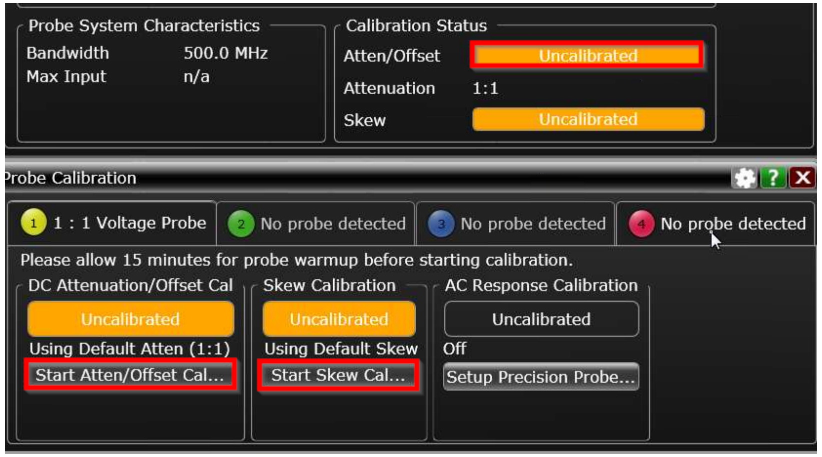
Probe Type Not Detected Automatically

Probe Type: Voltage Probe attached

Default Attenuation: 1.0000 : 1

Gain: ● Ratio ○ Decibel





Probe System Characteristics

Bandwidth	500.0 MHz
Max Input	n/a

Calibration Status

Atten/Offset	Uncalibrated
Attenuation	1:1
Skew	Uncalibrated

Probe Calibration

1 1 : 1 Voltage Probe | 2 No probe detected | 3 No probe detected | 4 No probe detected

Please allow 15 minutes for probe warmup before starting calibration.

DC Attenuation/Offset Cal	Skew Calibration	AC Response Calibration
Uncalibrated	Uncalibrated	Uncalibrated
Using Default Atten (1:1)	Using Default Skew	Off
Start Atten/Offset Cal...	Start Skew Cal...	Setup Precision Probe...

电缆De-Skew的连接

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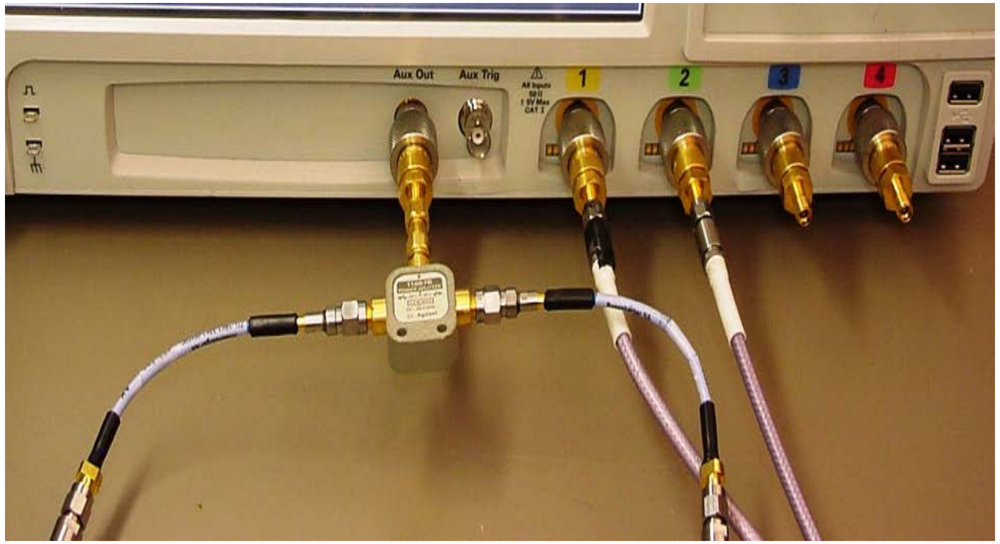
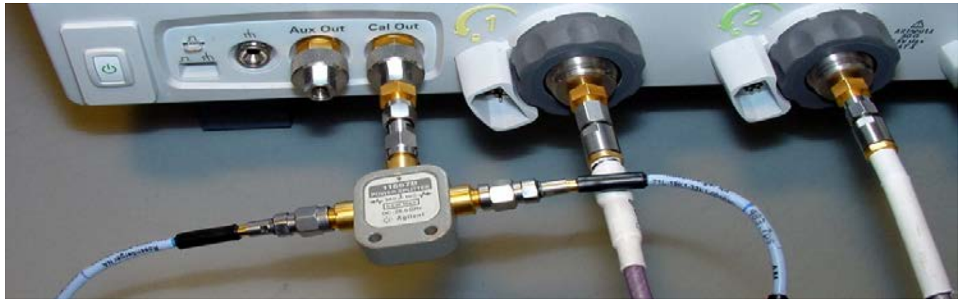
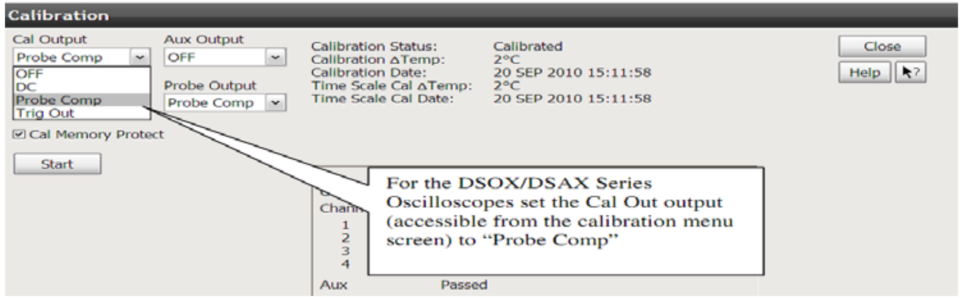
DSA90000A示波器De-Skew连接


Aux Out
Aux Trig
1
2
3
4

DSAX90000A示波器De-Skew连接示波器Utility—Calibration---Cal Output设置为Probe Comp


Aux Out
Cal Out
1
2


Calibration

Cal Output: Probe Comp
OFF
DC
Probe Comp
Trig Out

Aux Output: OFF

Probe Output: Probe Comp

☑ Cal Memory Protect

Calibration Status: Calibrated
Calibration ΔTemp: 2°C
Calibration Date: 20 SEP 2010 15:11:58
Time Scale Cal ΔTemp: 2°C
Time Scale Cal Date: 20 SEP 2010 15:11:58

Aux Passed

For the DSOX/DSAX Series Oscilloscopes set the Cal Out output (accessible from the calibration menu screen) to “Probe Comp”
Close
Help
Start
Chann
1
2
3
4

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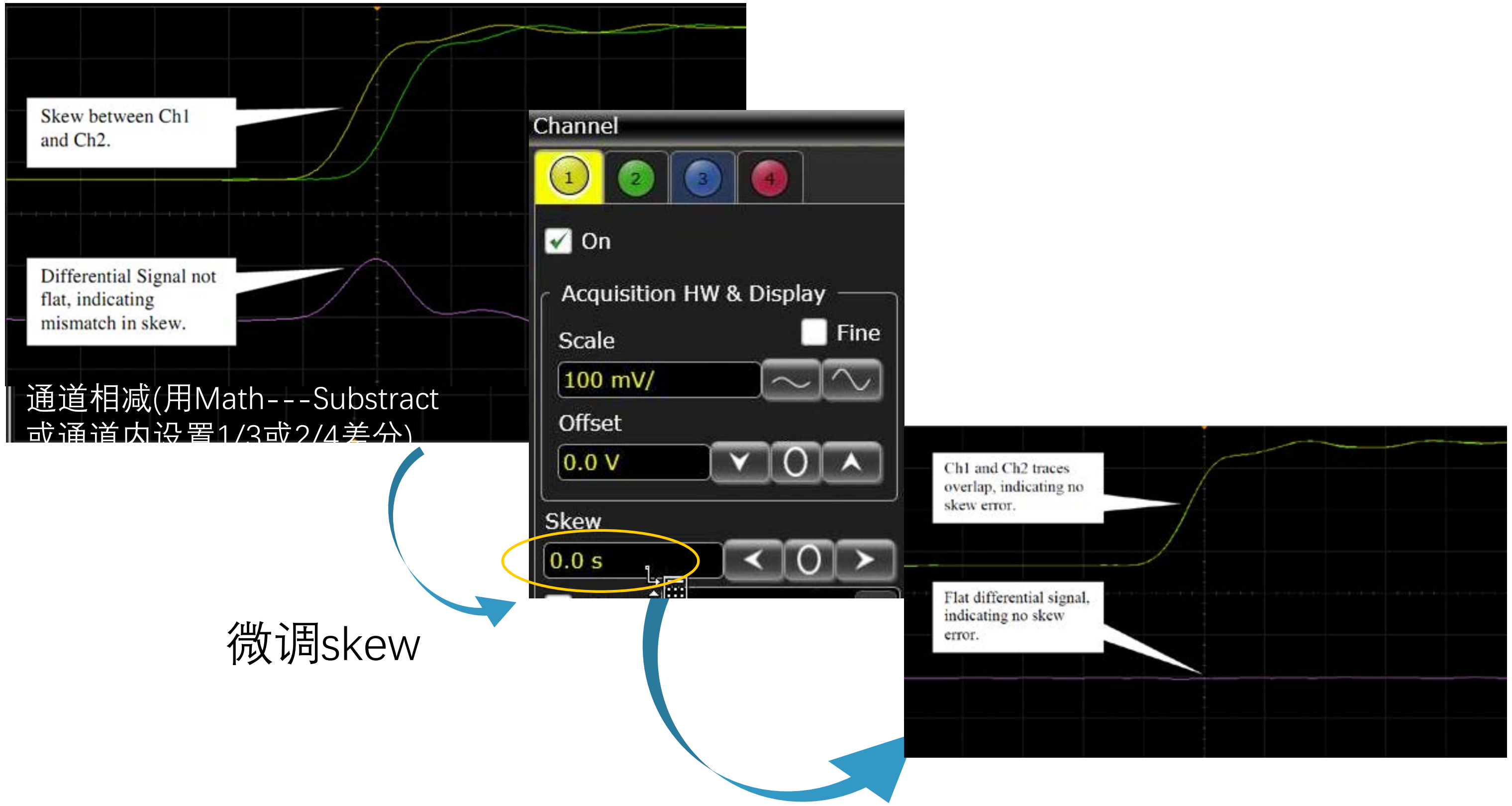
电缆De-Skew 调整

在示波器软件里File—Load—Setup调用INF_SMA_Deskew.set，或者用channel1上升沿触发，调整触发电平在-100多mV，水平时基设置为100ps/div，Setup---Acquisition---Average设置为16


Skew between Ch1 and Ch2.
Differential Signal not flat, indicating mismatch in skew.
Channel
1
2
3
4
Acquisition HW & Display
Ch1 and Ch2 traces overlap, indicating no skew error.
Flat differential signal, indicating no skew error.

☑ On

Scale 100 mV/ ☐ Fine

Offset 0.0 V

Skew 0.0 s

通道相减(用Math---Substract或通道内设置1/3或2/4差分)

微调skew

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