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Keysight MIPI C-PHY Physical Layer test solution

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BY
NeuHelium

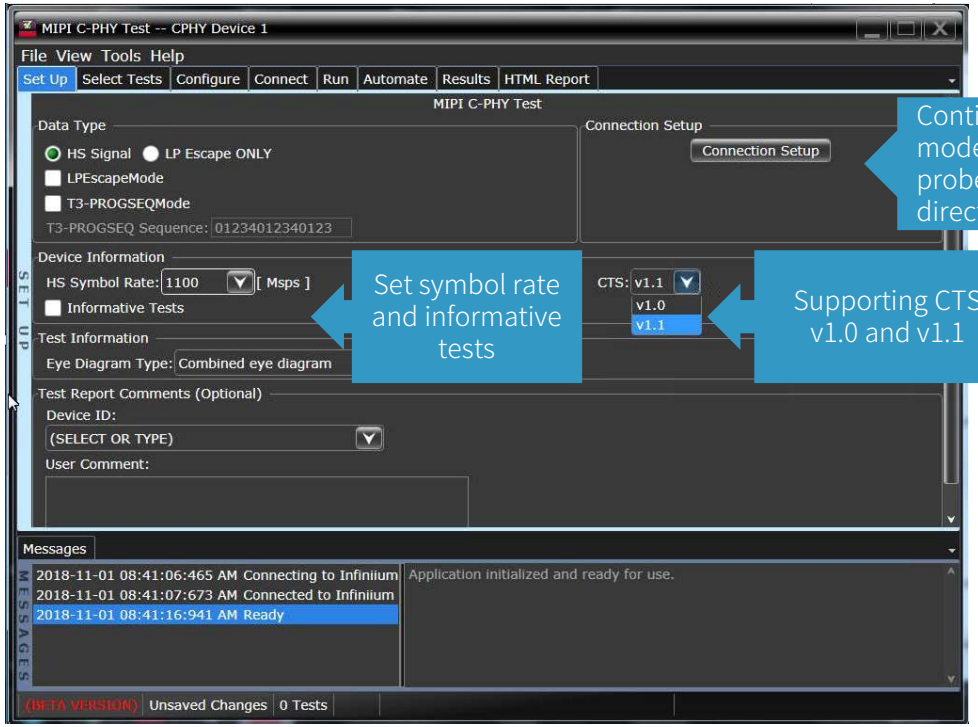
Agenda

Transmitter Testing

Receiver Testing

Keysight U7250A C-PHY Tx test software

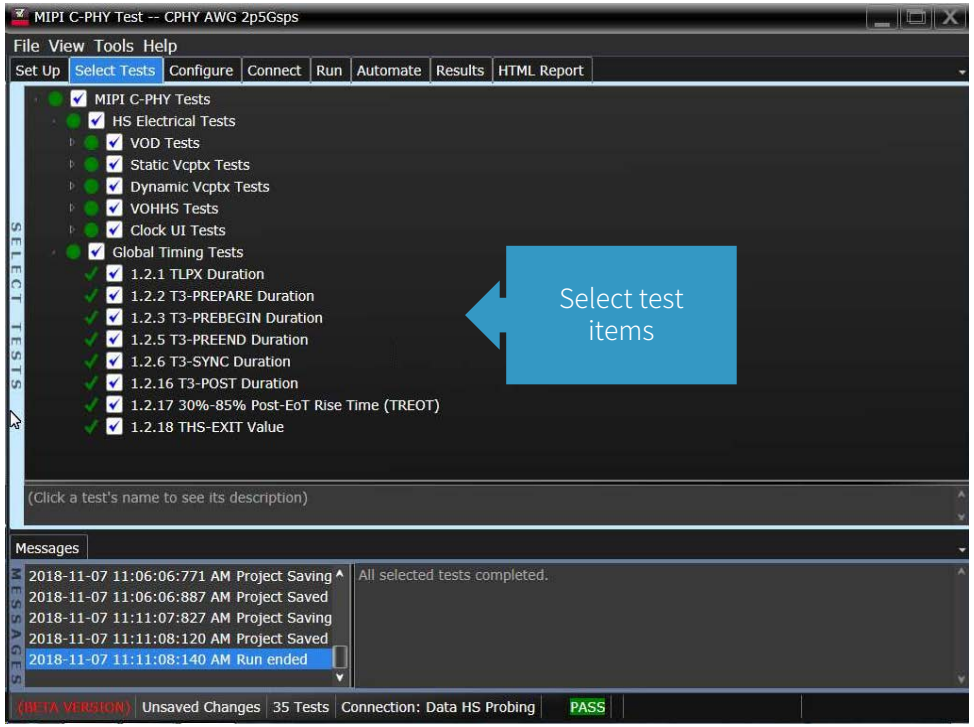
Outlook



Continuous and Burst mode support by Active probe connection and direct connection

Set symbol rate and informative tests

Supporting CTS v1.0 and v1.1



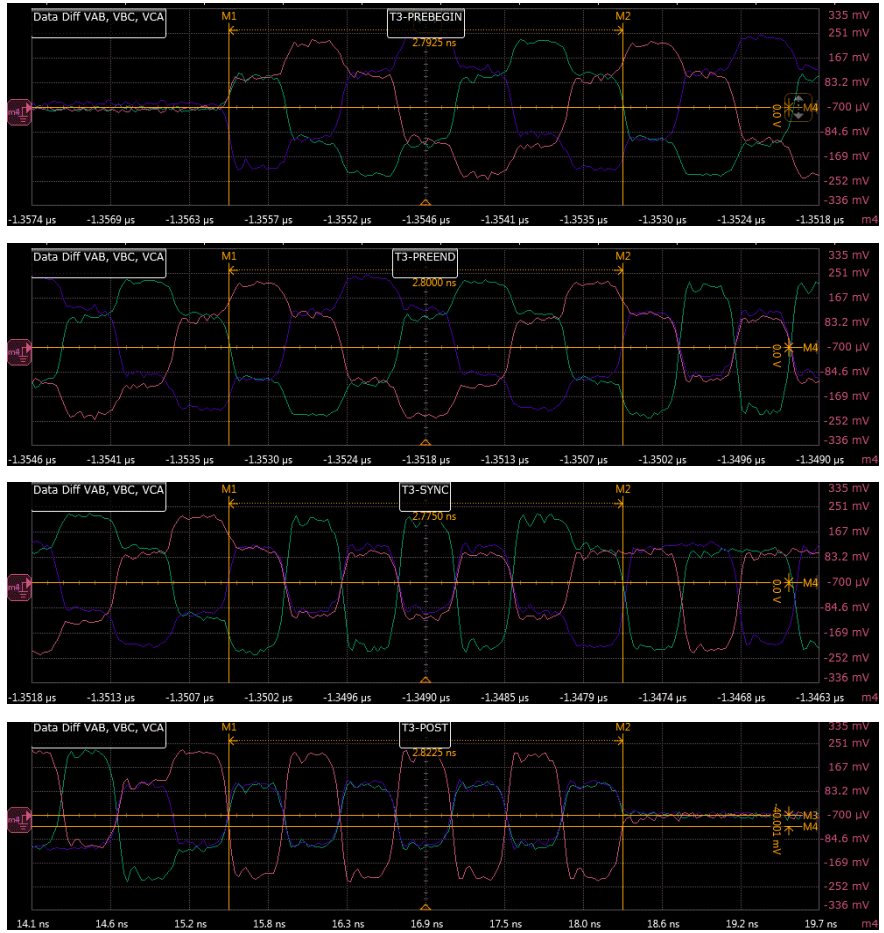
Select test items

Keysight U7250A C-PHY Tx test software

Test item Supporting

	CTS Test ID	Test Name	Test ID	Test Availability [CPHY v1.0]	C-PHY v1.1				
		Connection type		1 or 2	1	2	3	4	Pattern
LP Tests	1.1.1	LP-TX Thevenin Output High Level Voltage (VOH) ESCAPEMODE	100	YES	YES				ULPS
		LP-TX Thevenin Output High Level Voltage (VOH)	101	YES	YES				ULPS
	1.1.2	LP-TX Thevenin Output Low Level Voltage (VOL) ESCAPEMODE	200	YES	YES				ULPS
		LP-TX Thevenin Output Low Level Voltage (VOL)	201	YES	YES				ULPS
	1.1.3	LP-TX 15%-85% Rise Time (TRLP) ESCAPEMODE	300	YES	YES				ULPS
	1.1.4	LP-TX 15%-85% Fall Time (TFLP) ESCAPEMODE	400	YES	YES				ULPS
		LP-TX 15%-85% Fall Time (TFLP)	401	YES	YES				ULPS
	1.1.5	LP-TX Slew Rate vs. CLOAD (RiseEdgeMax)	500	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (RiseEdgeMin)	501	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (RiseEdgeMargin)	502	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (FallEdgeMax)	503	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (FallEdgeMin)	504	YES	YES				ULPS
	1.1.6	LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX)	600	YES	YES				ULPS
		LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX) [Initial]	601	YES	YES				ULPS
	1.1.7	LP-TX Period of Exclusive-OR Clock (TLP-PER-TX) [Rising-to-Rising]	700	YES	YES				ULPS
		LP-TX Period of Exclusive-OR Clock (TLP-PER-TX) [Falling-to-Falling]	701	YES	YES				ULPS
HS Electrical Tests	1.2.7	HS-TX Differential Voltages (VOD-AB-Strong1) [Max]	1700	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-AB-Weak1) [Min]	1701	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-AB-Weak0) [Max]	1702	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-AB-Strong0) [Min]	1703	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-BC-Strong1) [Max]	1710	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-BC-Weak1) [Min]	1711	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-BC-Weak0) [Max]	1712	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-BC-Strong0) [Min]	1713	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-CA-Strong1) [Max]	1720	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-CA-Weak1) [Min]	1721	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-CA-Weak0) [Max]	1722	YES			YES	YES	Cont
		HS-TX Differential Voltages (VOD-CA-Strong0) [Min]	1723	YES			YES	YES	Cont
	1.2.8	HS-TX Differential Voltage Mismatch (ΔVOD)	1800	YES			YES	YES	Cont
	1.2.9	HS-TX Single-Ended Output High Voltages (VOHHS(VA))	1900	YES			YES	YES	Cont
		HS-TX Single-Ended Output High Voltages (VOHHS(VB))	1901	YES			YES	YES	Cont
		HS-TX Single-Ended Output High Voltages (VOHHS(VC))	1902	YES			YES	YES	Cont
	1.2.10	HS-TX Static Common-Point Voltages (VCPTX_HS_+X)	2000	YES			YES	YES	Cont
		HS-TX Static Common-Point Voltages (VCPTX_HS_-X)	2001	YES			YES	YES	Cont
		HS-TX Static Common-Point Voltages (VCPTX_HS_+Y)	2002	YES			YES	YES	Cont
		HS-TX Static Common-Point Voltages (VCPTX_HS_-Y)	2003	YES			YES	YES	Cont
		HS-TX Static Common-Point Voltages (VCPTX_HS_+Z)	2004	YES			YES	YES	Cont
		HS-TX Static Common-Point Voltages (VCPTX_HS_-Z)	2005	YES			YES	YES	Cont
	1.2.11	HS-TX Static Common-Point Voltage Mismatch (ΔVCPTX(HS))	2100	YES			YES	YES	Cont
	1.2.12	HS-TX Dynamic Common-Point Variations Between 50-450MHz (ΔVCPTX(LF))	2200	YES			YES	YES	Cont
	1.2.13	HS-TX Dynamic Common-Point Variations Above 450MHz (ΔVCPTX(HF))	2300	YES			YES	YES	Cont
	1.2.14	HS-TX Rise Time (tR) [1.5Gbps and below]	2400	YES			Infor	Infor	Cont
		HS-TX Rise Time (tR) [above 1.5Gbps]	2401	YES			Infor	Infor	Cont
	1.2.15	HS-TX Fall Time (tF) [1.5Gbps and below]	2500	YES			Infor	Infor	Cont
		HS-TX Fall Time (tF) [above 1.5Gbps]	2501	YES			Infor	Infor	Cont
	1.2.19	HS Clock Instantaneous UI (UIINST_Max)	2900	YES			YES	YES	Cont
	1.2.20	HS Clock Delta UI (ΔUI) [1Gbps and below]	3000	YES			YES	YES	Cont
		HS Clock Delta UI (ΔUI) [above 1Gbps]	3001	YES			YES	YES	Cont
	1.2.21	HS-TX Eye diagram					YES	YES	Cont
HS Timing Tests	1.2.1	TLPX Duration	1100	YES		YES			Burst
	1.2.2	T3-PREPARE Duration	1200	YES		YES			Burst
	1.2.3	T3-PREBEGIN Duration	1300	NO		YES			Burst
	1.2.4	T3-PROGSEQ Duration	1400	NO		YES			Burst
	1.2.5	T3-PREEND Duration	1500	NO		YES			Burst
	1.2.6	T3-SYNC Duration	1600	NO		YES			Burst
	1.2.16	T3-POST Duration	2600	NO		YES			Burst
	1.2.18	THS-EXIT Value	2800	YES		YES			Burst
	1.2.17	30%-85% Post-EoT Rise Time (TREOT)	2700	YES		YES			Burst

Enabled Protocol Related Test item

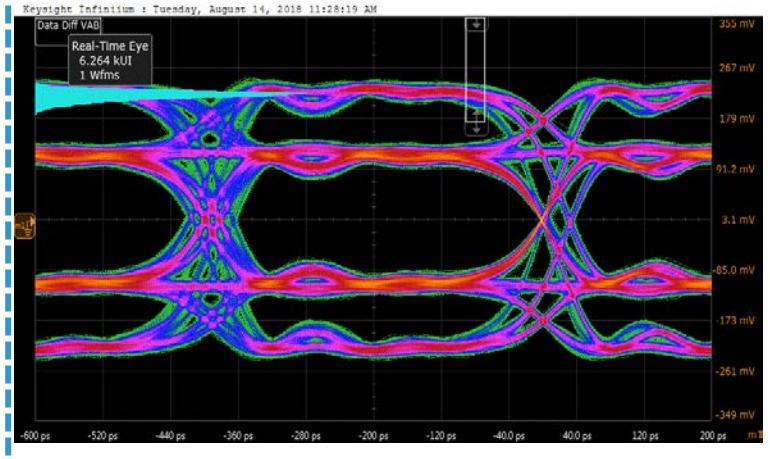


Keysight U7250A C-PHY Tx test software

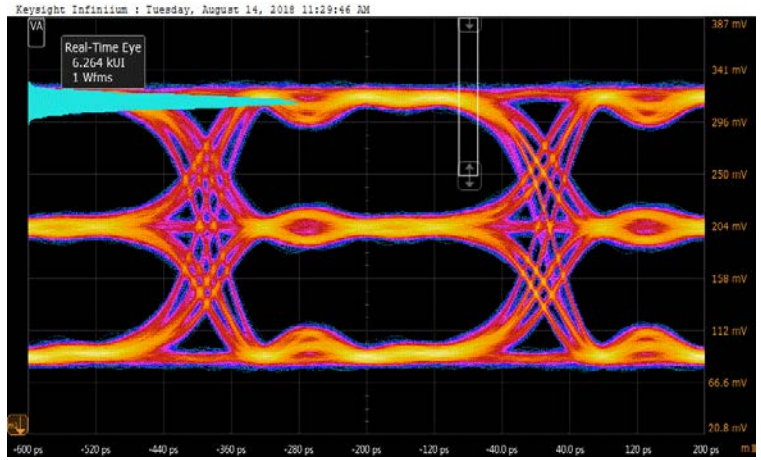
Test result example

U7250A

1.2.7 HS-TX Differential Voltages (VOD-AB, VOD-BC, VOD-CA)



1.2.9 HS-TX Single-Ended Output High Voltages (VOHHS(VA), VOHHS(VB), VOHHS(VC))



CTS simulation

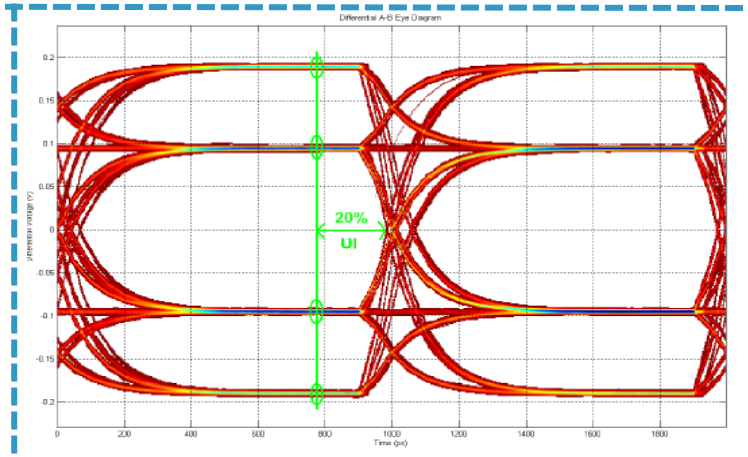
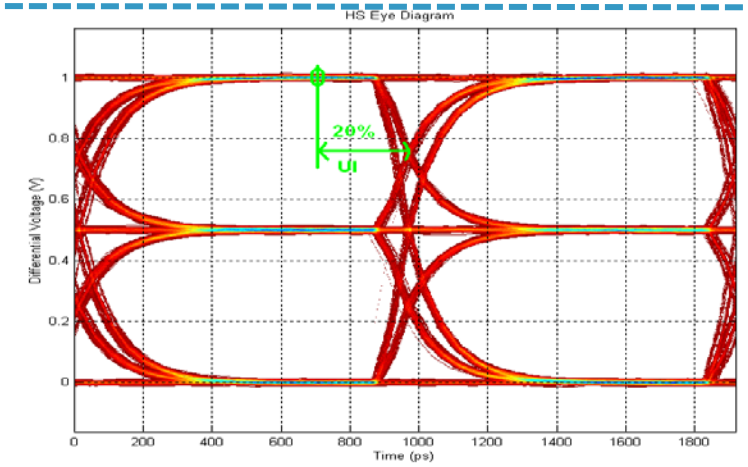
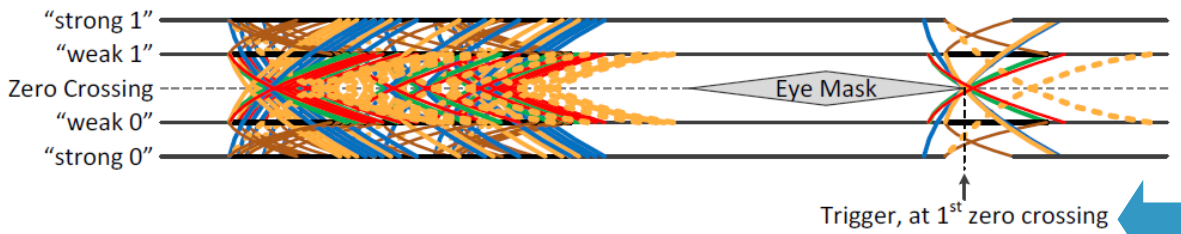


Figure 1.2.7-3: Sample V_{OD} Measurement at 20% UI Width



Keysight U7250A C-PHY Tx test software

Clock recovery



Clock is recovered from the earliest edge of a symbol transition.

Figure 63 C-PHY Eye Pattern Example, Triggered Eye

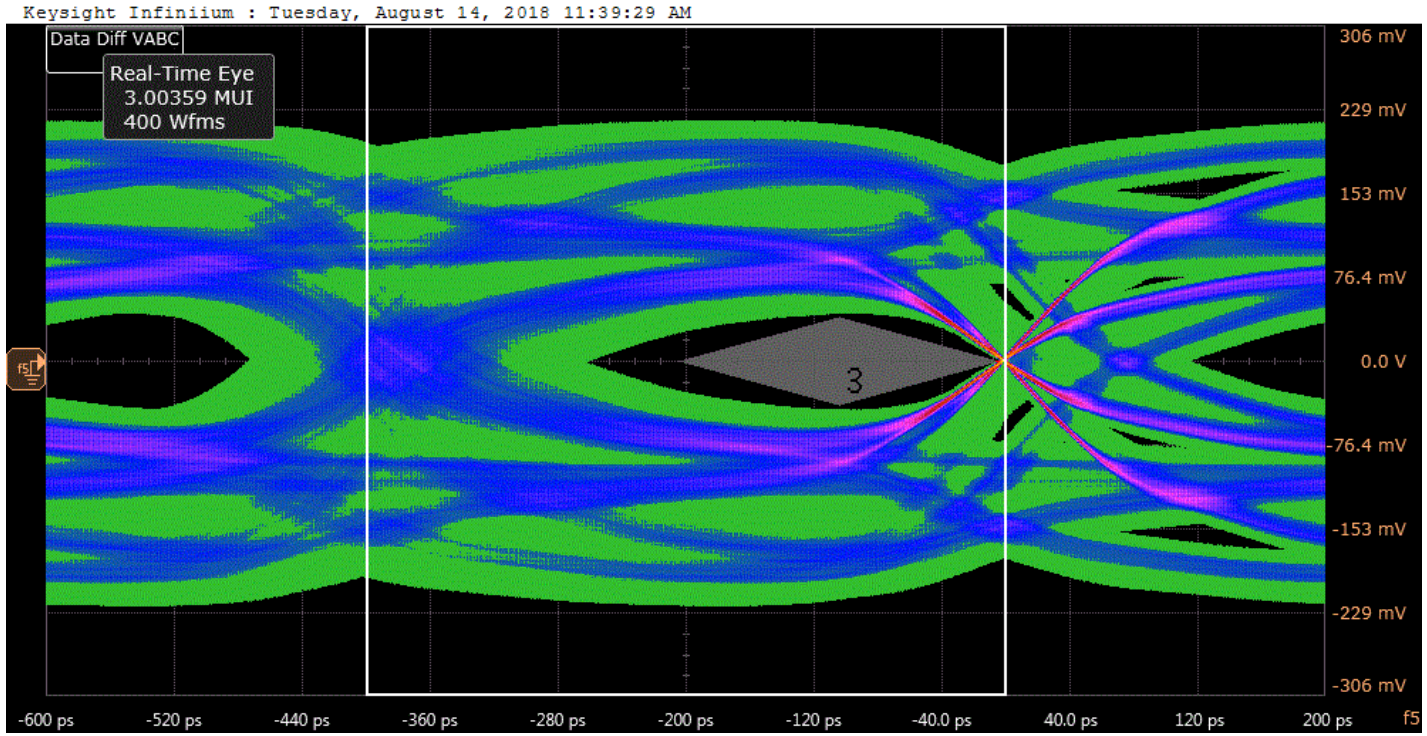
2. Using function make VAB, VAC, VBC (Symbol transition)

3. Among VAB, VAC, VBC, find each first arrival edge on acquired signal and build clock recovery

1. Acquire VA, VB, VC at once

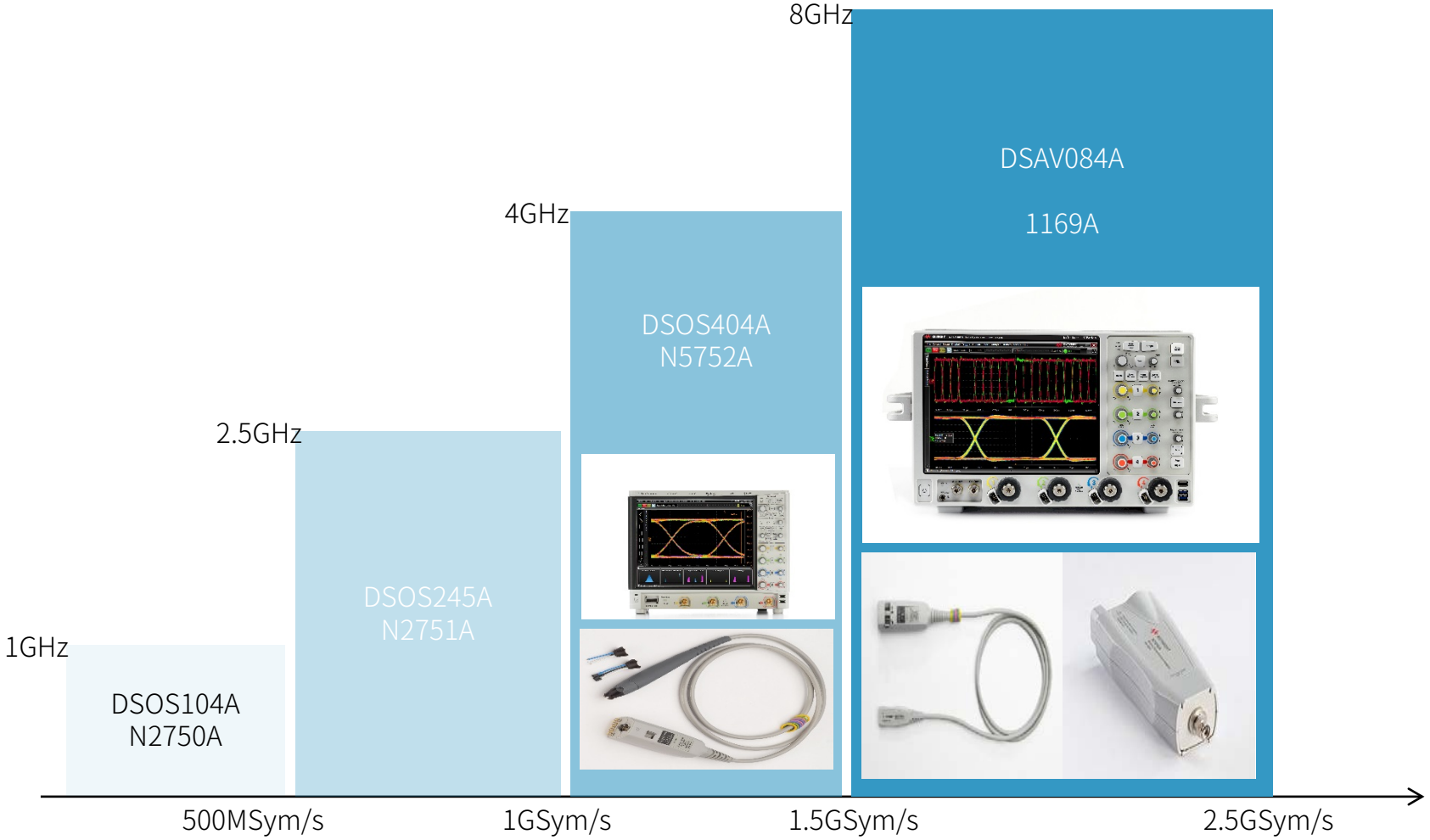
Keysight U7250A C-PHY Tx test software

Eye diagram Test result example



Test 1.2.21 Eye diagram test example with Standard channel embedding

Keysight Solutions for MIPI TX PHY-test



MIPI TX Test Solutions

Product Number

	<500MSym/s	<1GSym/s	<1.5GSym/s	≤ 2.5GSym/s
Oscilloscope	DSOS104A	DSOS254A	DSOS404A	DSAV804A
Probe	N2750A : 1.5GHz active probe x3	N2751A : 3.5GHz active probe x3	N2752A : 6GHz active probe x3	1169A : 12GHz active probe x3 And N7010A : active termination adapter x3
Software	U7250A : MIPI C-PHY conformance test application E2688A : Serial data analysis/mask testing with clock recovery N5414B : InfiniiScan software N5465B : InfiniiSim waveform transformation toolset			

Oscilloscope base line software must be same or above 6.20

Agenda

Transmitter Testing

Receiver Testing

About Receiver (RX) testing

RX testing

An RX test is used to determine an RX’ s capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing…

- A Bit Error Ratio Tester’ s (BERT) Pattern Generator (BERT PG) is used to emulate a system’ s TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.
  This signal has to be calibrated according to the specification
- The input of the RX under test is stimulated with this signal
- Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

Jitter Tolerance Calibration and Measurement

- Calibrate the Rise/Fall times from the test equipment generator to approx. 115ps using 20%-80% transition time converter
- Calibrate the Eye width of three differential signals A-B, B-C, A-C to be 0.7UI by adding Jitter (e.g. DCD) over the already present switching jitter, of course using proper C-PHY clock recovery algorithm.
- Add ISI jitter by either using a HW channel or SW-programming of the generator to meet the 0.3UI of channel ISI requirement.
- Tune the Amplitude and the amount of ISI to meet the eye mask requirement of +40 to -40mV for EH and 0.4UI for EW.
  (Allow 10% of variation in calibration over the time scale wrt. the targeted eye mask spec.)
- After generating the worst case eye as per the mask requirements, Check for any errors in the receiver by comparing the received pattern with the receiver expected pattern and varying DC Common mode.

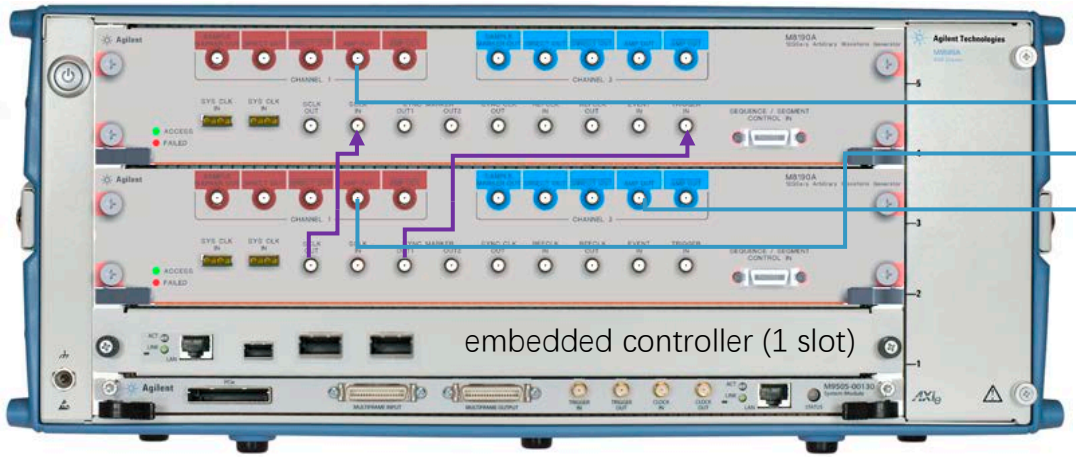
How to Test MIPI C- /D-PHY RXs acc. to CTS?

Keysight M8000 Series of BER Test Solutions!

- Modular system in AXI form factor consisting of
  - AWG modules M8190/95A
    (used for multilevel and non-NRZ signals)
  - BERT modules M8041A and M8051A
    (used for two level, NRZ (and similar) signals)
  - plus M8070A SW with application plug ins (e.g. M8085 for MIPI)
  - Keysight J-BERT M8020A (=M8041/51A +M8070A SW)
    - modular up to 4 channels
      enabling channel skew measurements
    - Very well suited for M-PHY
    - Very much comparable to N4903
- Test Automation SW: Keysight N5990A
  - option 165 & 365 for MIPI M-PHY
    using w/ J-BERT M8020A or N4903B

Setup for C-PHY, single lane:

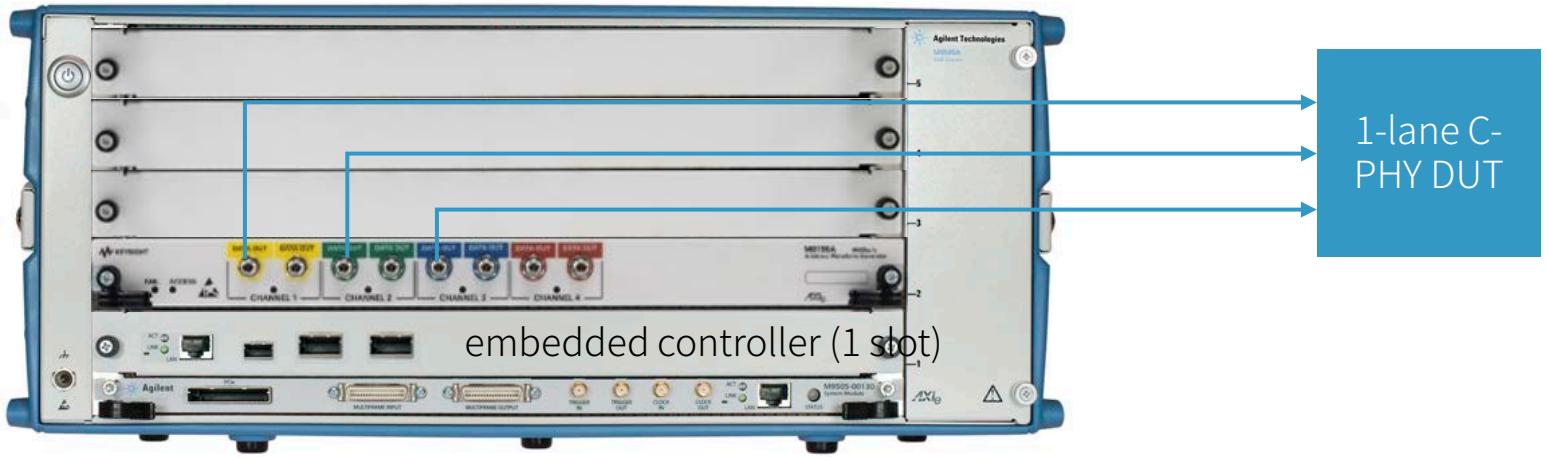
M8190A, 5 Slot Frame, Embedded Controller



1-lane C-PHY DUT

Setup for C-PHY, single lane:

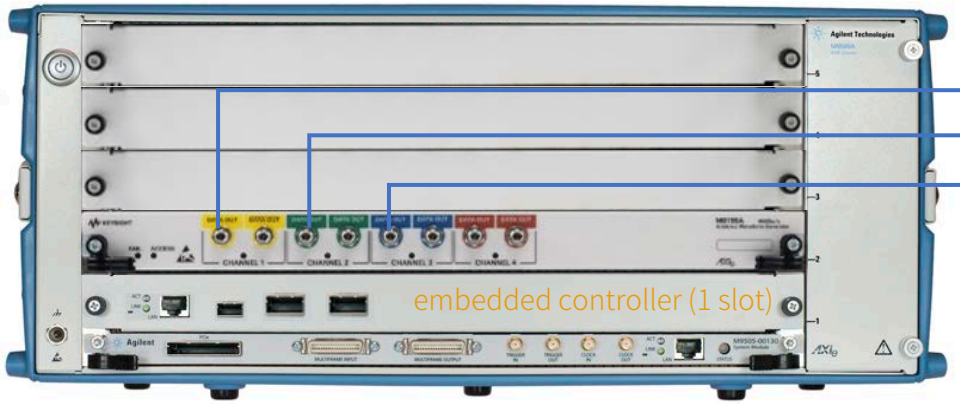
M8195A, 5 Slot Frame, Embedded Controller



4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)

Setup for C-PHY, single lane:

M8195A, 5 Slot Frame, Embedded Controller



1-lane C-PHY DUT

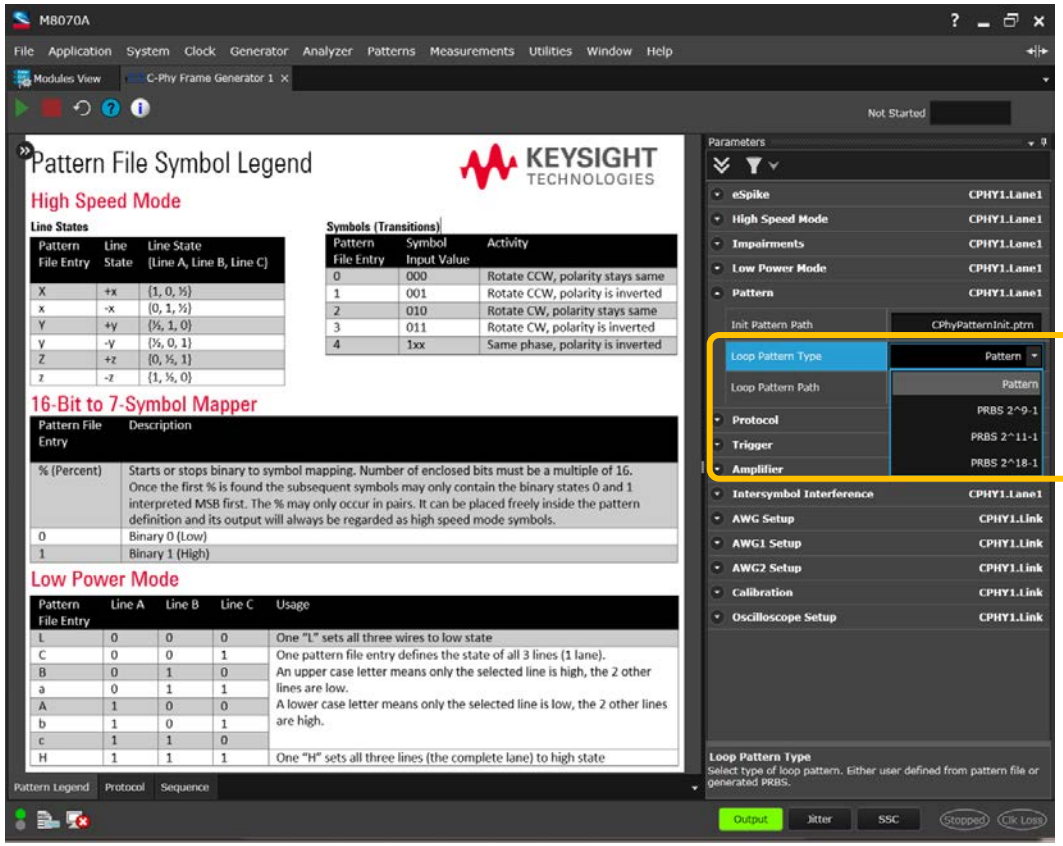
4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)

Alternative setup: M8195A, 2 slot frame, embedded Controller

1-lane C-PHY DUT

Realization of "C-PHY-editor “ within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW



HS-Pattern can be set up as

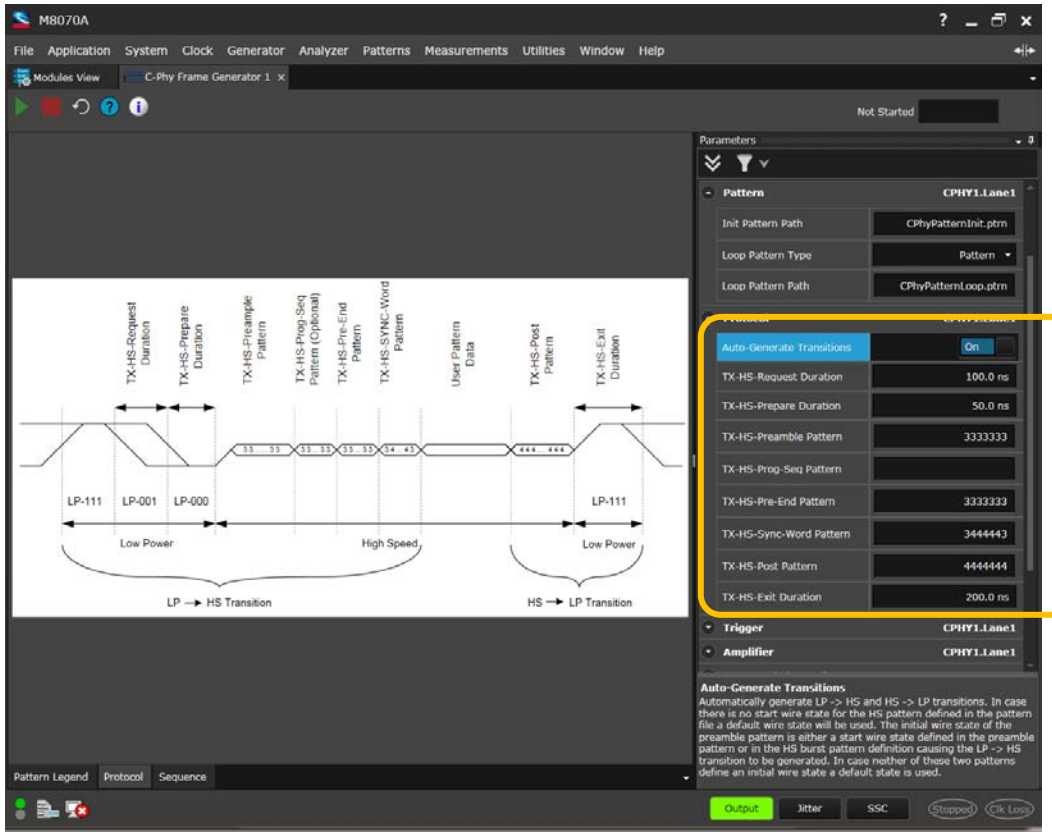
- Serial data
  (encoder is integrated)
- Symbol value (0,1,2,3,4)
- Wire state (+/- x,y,z)
- Predefined PRBS

LS-Pattern
(8 possible states)

- can be set up as symbols
  (L, H, a, A, b, B, c, C)

Realization of "C-PHY-editor “ within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW

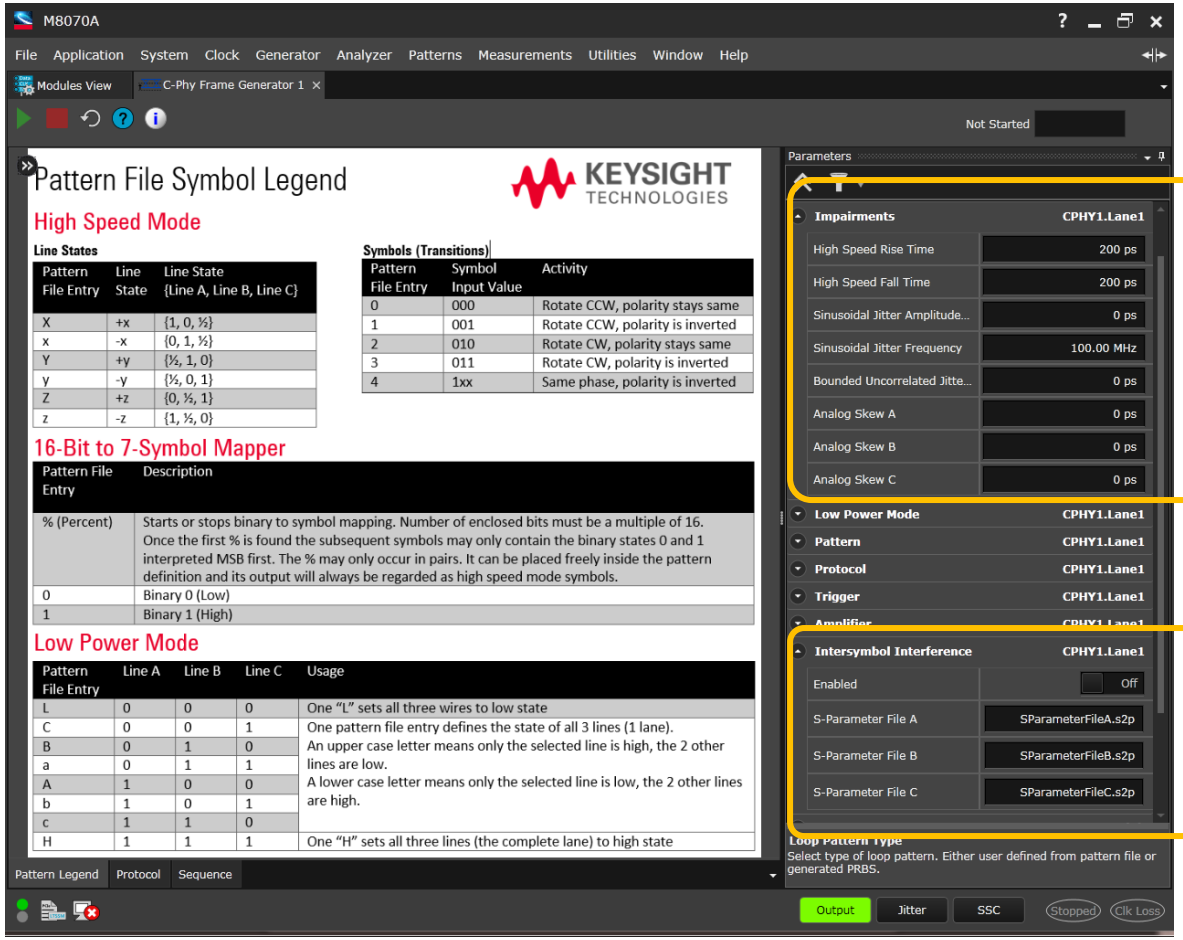


Set up of a sequence with LP - HS patterns, transition generated automatically

Parameters and patterns can be edited

Realization of "C-PHY-editor “ within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW

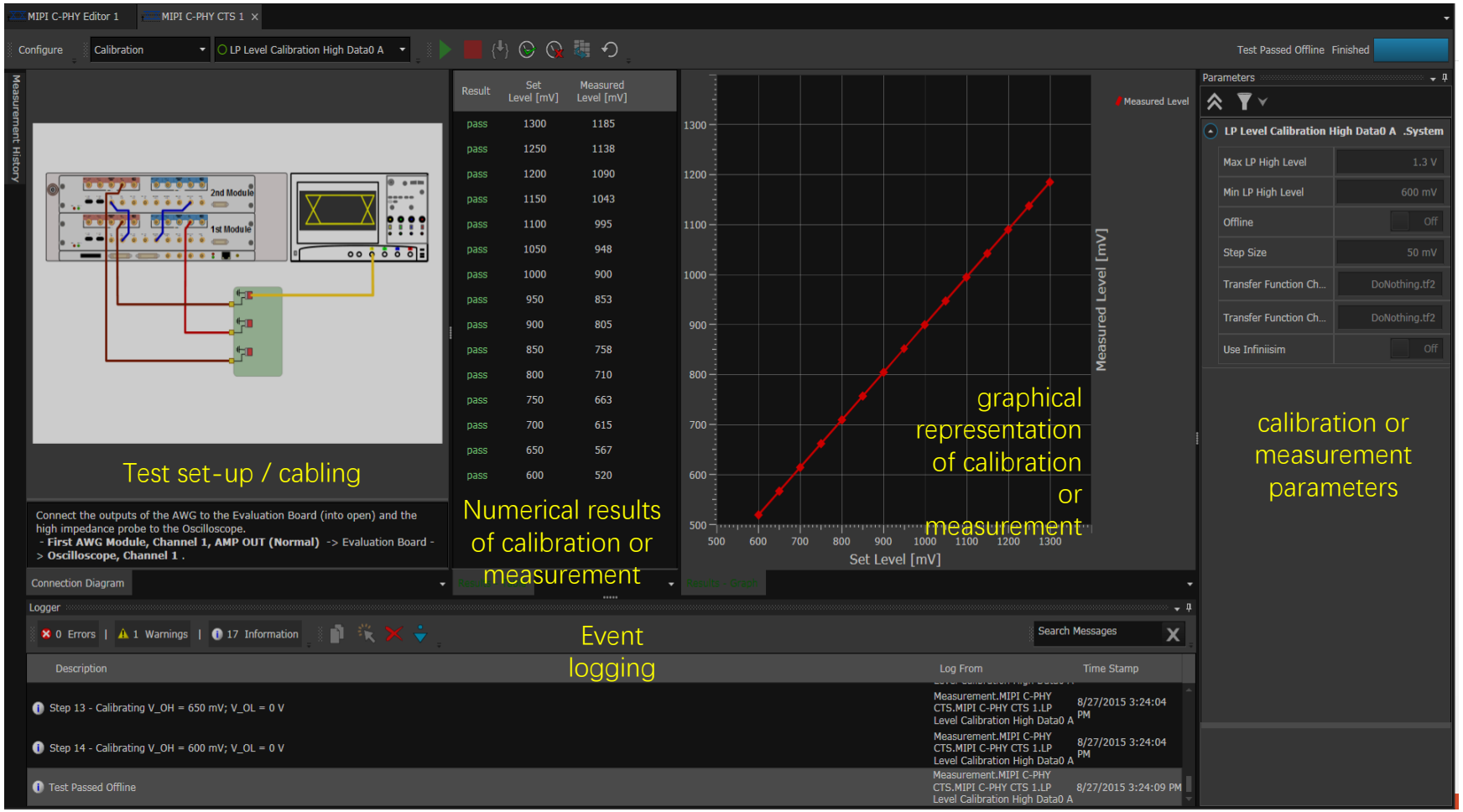


Set-up of parameters in a BERT-like fashion

HS-impairments

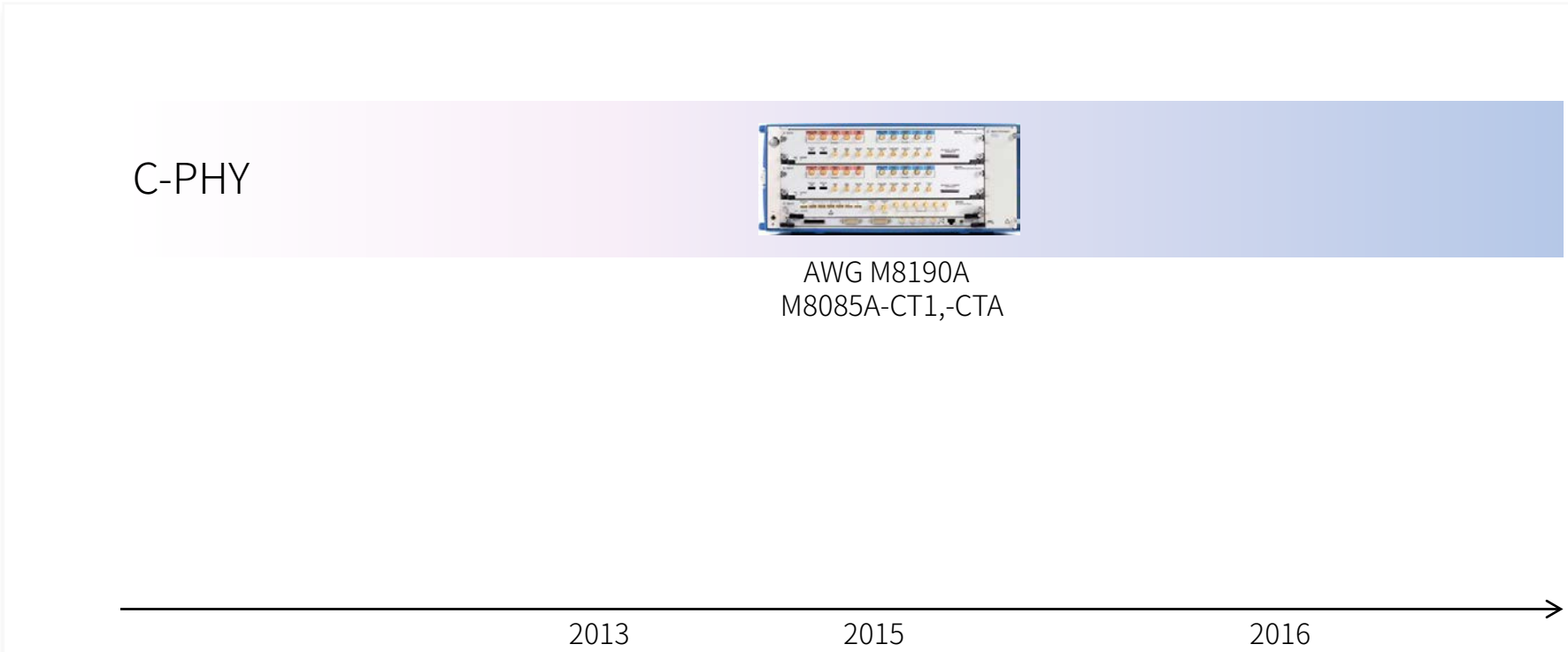
ISI via S-parameters

GUI for C-PHY CTS Calibration and Test Procedures



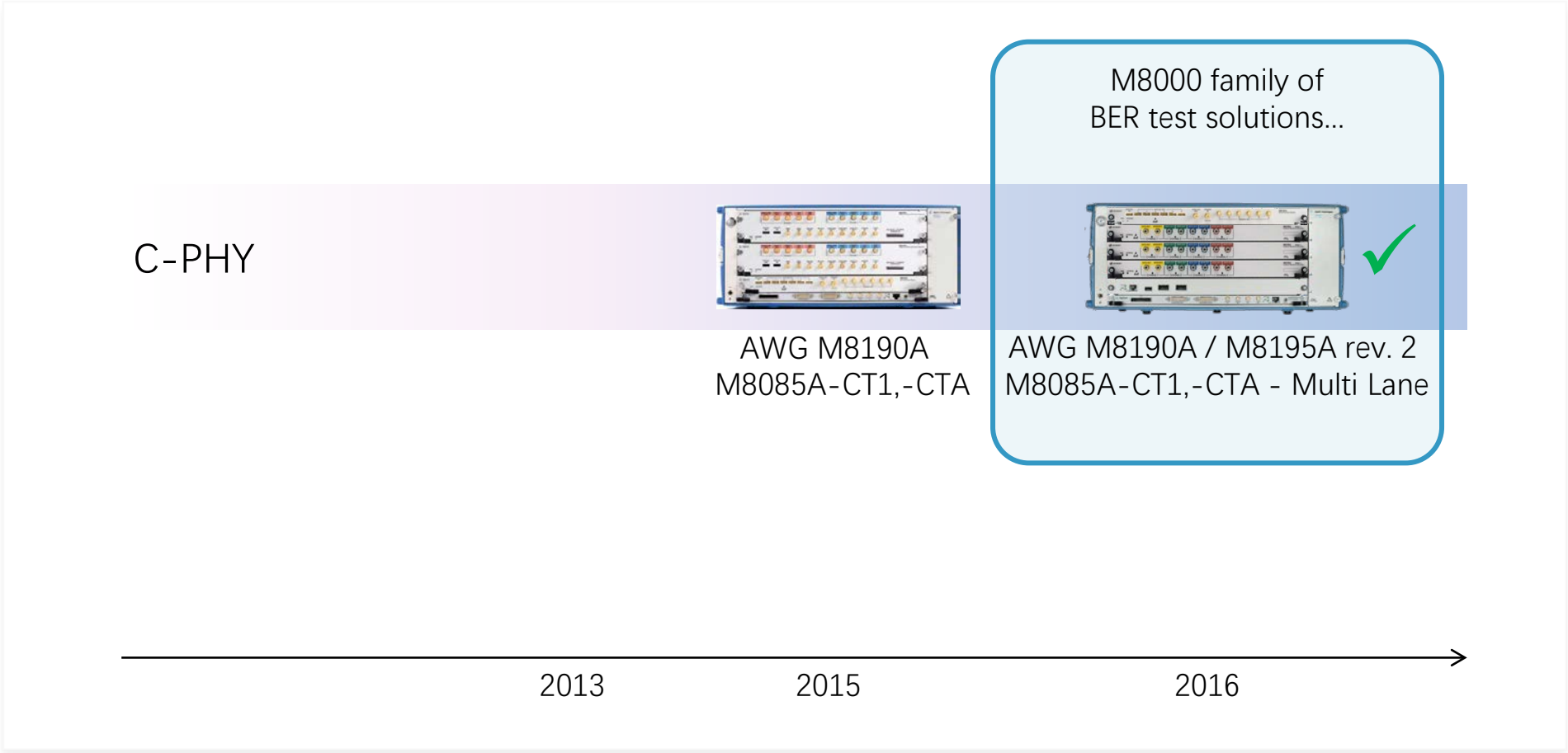
Keysight Solutions for MIPI RX PHY-test

2015: M8085A w/ M8190A addressing C-PHY



Keysight Solutions for MIPI RX PHY-test

2016 and beyond: M8085A w/ M8195A rev. 2

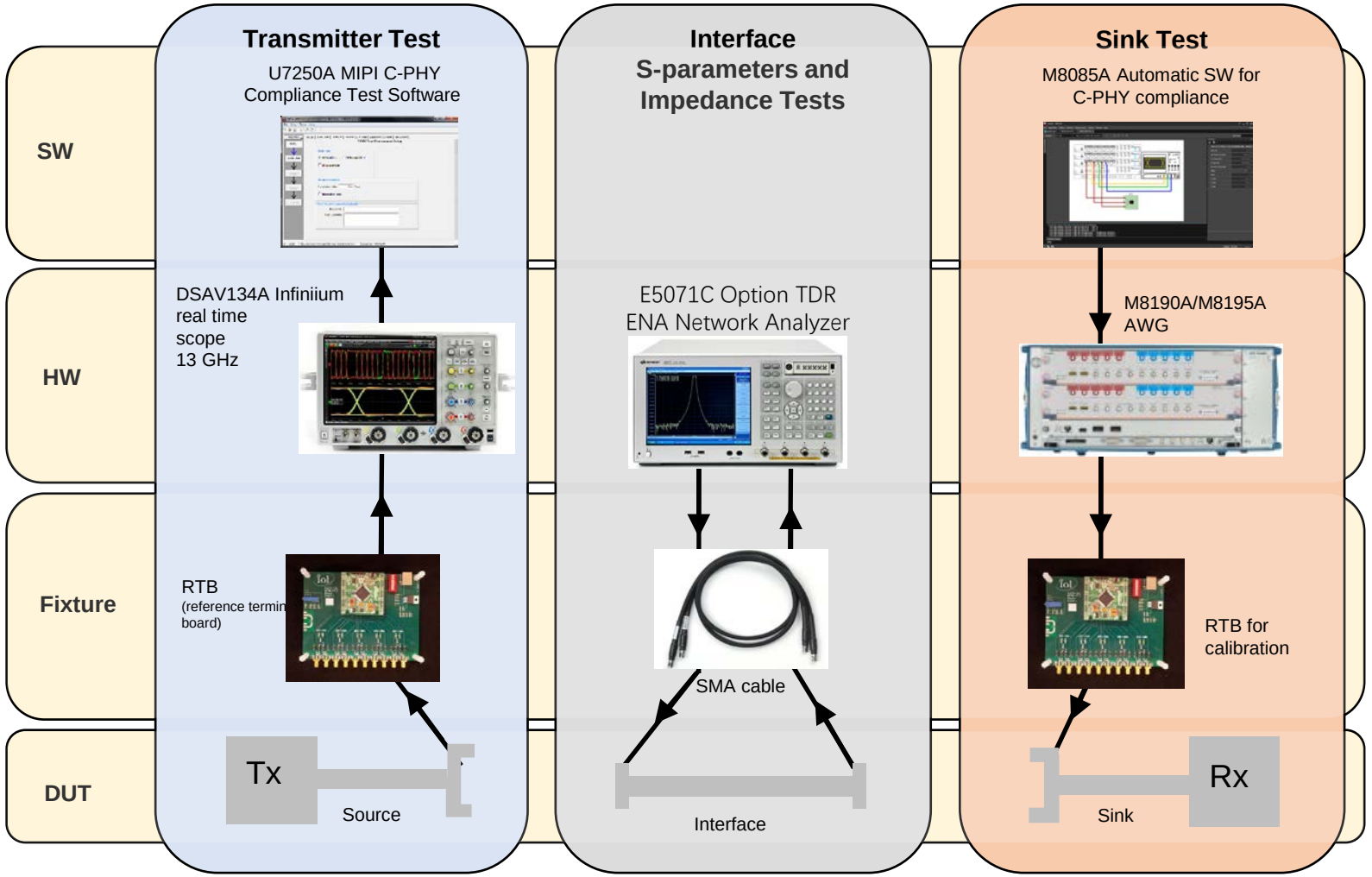


MIPI RX Test Solutions

Availability and Product / Option Number

	M8085A	
Instrument / HW	**M8190A**	**M8195A, rev. 2**
Link-type	**Single-lane**	**Multi-lane**
C-PHY	N5990A-010, CT1, CTA Sept. 2015	N5990A-010, CT1, CTA Q2FY2016
	M8070A rev 3.0 or higher is required to host the M8085A PlugIns All “T“ licenses also available as “N“ = network license	

Keysight MIPI C-PHY Solution Coverage

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