

# Keysight MIPI C-PHY Physical Layer test solution

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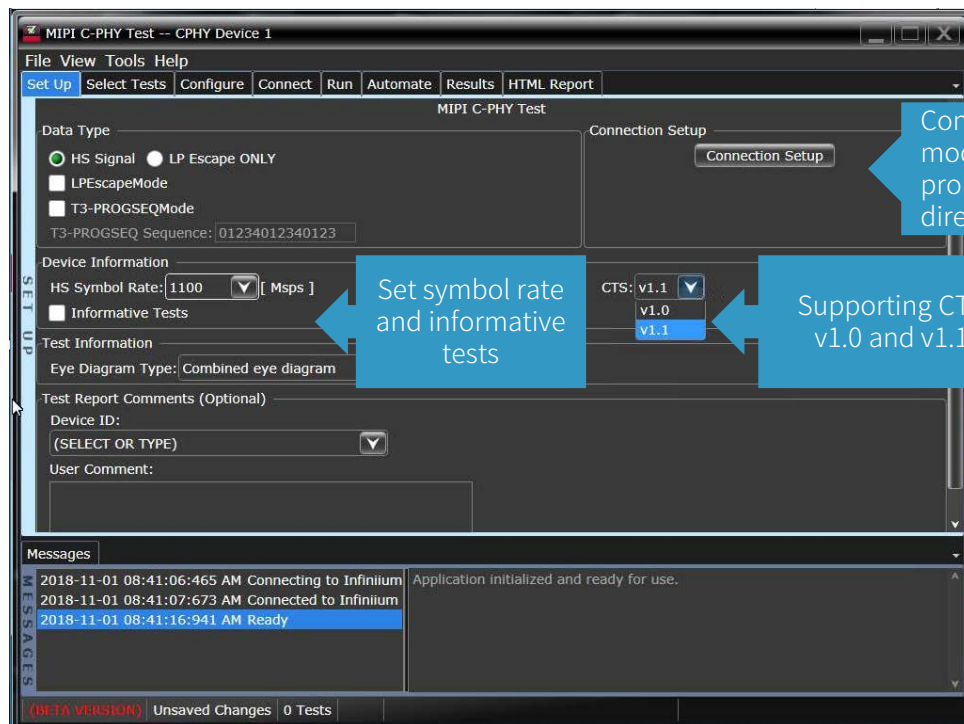
# Agenda

Transmitter Testing

Receiver Testing

# Keysight U7250A C-PHY Tx test software

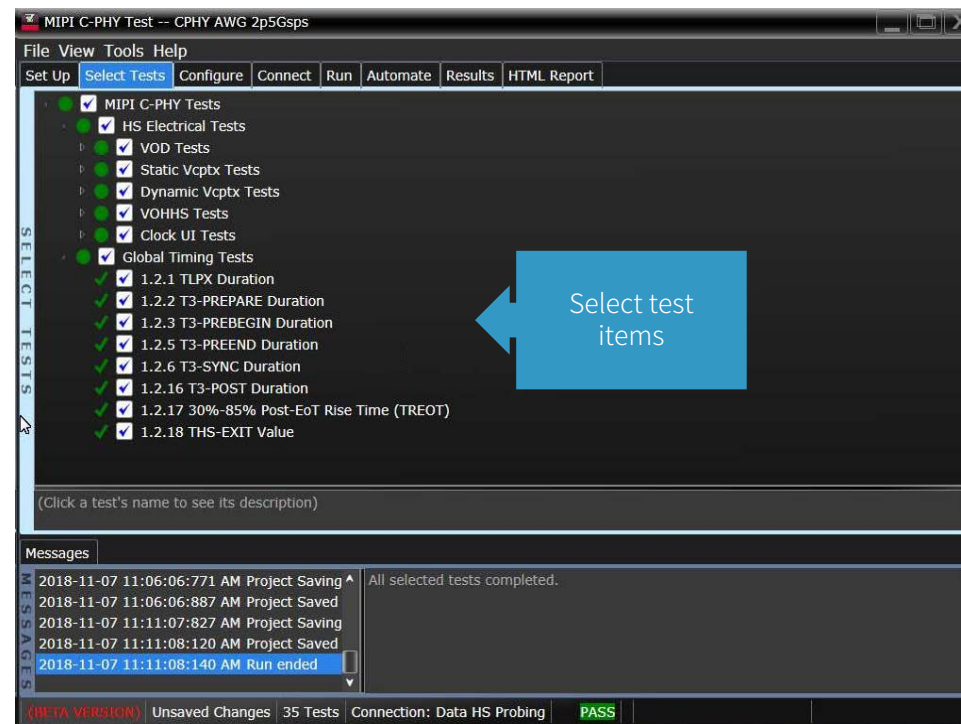
## Outlook



Continuous and Burst mode support by Active probe connection and direct connection

Set symbol rate and informative tests

Supporting CTS v1.0 and v1.1



Select test items

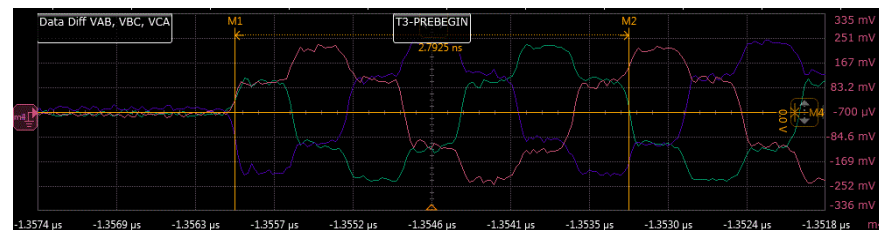
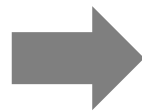
# Keysight U7250A C-PHY Tx test software

## Test item Supporting

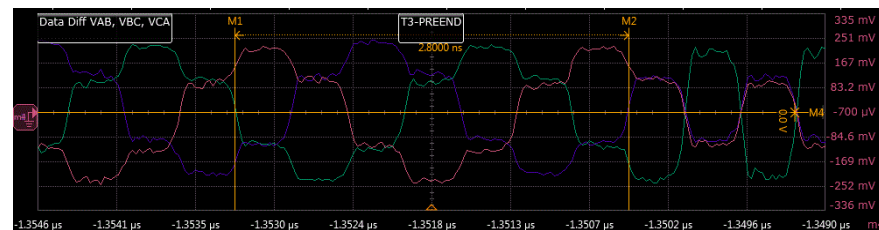
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CTS Test ID	Test Name	Test ID	Test Availability [CPHY v1.0]	C-PHY v1.1					
				1 or 2	1	2	3	4	Pattern
Connection type									
LP Tests	1.1.1	LP-TX Thevenin Output High Level Voltage (VOH) ESCAPEMODE	100	YES	YES				ULPS
		LP-TX Thevenin Output High Level Voltage (VOH)	101	YES	YES				ULPS
	1.1.2	LP-TX Thevenin Output Low Level Voltage (VOL) ESCAPEMODE	200	YES	YES				ULPS
		LP-TX Thevenin Output Low Level Voltage (VOL)	201	YES	YES				ULPS
	1.1.3	LP-TX 15%-85% Rise Time (TR15) ESCAPEMODE	300	YES	YES				ULPS
	1.1.4	LP-TX 15%-85% Fall Time (TFLP) ESCAPEMODE	400	YES	YES				ULPS
		LP-TX 15%-85% Fall Time (TFLP)	401	YES	YES				ULPS
	1.1.5	LP-TX Slew Rate vs. CLOAD (RiseEdgeMax)	500	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (RiseEdgeMin)	501	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (FallEdgeMargin)	502	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (FallEdgeMax)	503	YES	YES				ULPS
		LP-TX Slew Rate vs. CLOAD (FallEdgeMin)	504	YES	YES				ULPS
	1.1.6	LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX)	600	YES	YES				ULPS
		LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX) [Initial]	601	YES	YES				ULPS
		LP-TX Period of Exclusive-OR Clock (TLP-PER-TX) [Rising-to-Rising]	700	YES	YES				ULPS
	1.1.7	LP-TX Period of Exclusive-OR Clock (TLP-PER-TX) [Falling-to-Falling]	701	YES	YES				ULPS
	HS Electrical Tests	1.2.7	HS-TX Differential Voltages (VOD-AB-Strong) [Max]	1700	YES		YES	YES	
		HS-TX Differential Voltages (VOD-AB-Weak) [Min]	1701	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-AB-Weak) [Max]	1702	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-AB-Strong) [Min]	1703	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-BC-Strong) [Max]	1710	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-BC-Weak) [Min]	1711	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-BC-Weak) [Max]	1712	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-BC-Strong) [Min]	1713	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-CA-Strong) [Max]	1720	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-CA-Weak) [Min]	1721	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-CA-Weak) [Max]	1722	YES		YES	YES		Cont
		HS-TX Differential Voltages (VOD-CA-Strong) [Min]	1723	YES		YES	YES		Cont
1.2.8		HS-TX Differential Voltage Mismatch (ΔVOD)	1800	YES		YES	YES		Cont
1.2.9		HS-TX Single-Ended Output High Voltages (VOHHS(VA))	1900	YES		YES	YES		Cont
	HS-TX Single-Ended Output High Voltages (VOHHS(VB))	1901	YES		YES	YES		Cont	
	HS-TX Single-Ended Output High Voltages (VOHHS(VC))	1902	YES		YES	YES		Cont	
1.2.10	HS-TX Static Common-Point Voltages (VCPTX_HS_-X)	2000	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltages (VCPTX_HS_-X)	2001	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltages (VCPTX_HS_-Y)	2002	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltages (VCPTX_HS_-Y)	2003	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltages (VCPTX_HS_-Z)	2004	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltages (VCPTX_HS_-Z)	2005	YES		YES	YES		Cont	
	HS-TX Static Common-Point Voltage Mismatch (ΔVCPTX[HS])	2100	YES		YES	YES		Cont	
1.2.11	HS-TX Dynamic Common-Point Variations Between 50-450MHz (ΔVCPTX[L])	2200	YES		YES	YES		Cont	
1.2.12	HS-TX Dynamic Common-Point Variations Above 450MHz (ΔVCPTX[H])	2300	YES		YES	YES		Cont	
1.2.13	HS-TX Rise Time (TR) [1.5Gbps and below]	2400	YES		Infor	Infor		Cont	
1.2.14	HS-TX Rise Time (TR) [above 1.5Gbps]	2401	YES		Infor	Infor		Cont	
	HS-TX Fall Time (TF) [1.5Gbps and below]	2500	YES		Infor	Infor		Cont	
1.2.15	HS-TX Fall Time (TF) [above 1.5Gbps]	2501	YES		Infor	Infor		Cont	
1.2.19	HS Clock Instantaneous UI (UIINST_Max)	2900	YES		YES	YES		Cont	
1.2.20	HS Clock Delta UI (ΔUI) [1Gbps and below]	3000	YES		YES	YES		Cont	
	HS Clock Delta UI (ΔUI) [above 1Gbps]	3001	YES		YES	YES		Cont	
1.2.21	HS-TX Eye diagram	1100	YES		YES	YES		Cont	
HS Timing Tests	1.2.1	T1X Duration	1100	YES		YES			Burst
	1.2.2	T3-PREPREP Duration	1200	YES		YES			Burst
	1.2.3	T3-PREBEGIN Duration	1300	NO		YES			Burst
	1.2.4	T3-PROGSEQ Duration	1400	NO		YES			Burst
	1.2.5	T3-PREEND Duration	1500	NO		YES			Burst
	1.2.6	T3-SYNC Duration	1600	NO		YES			Burst
	1.2.16	T3-POST Duration	2600	NO		YES			Burst
	1.2.18	THS-EXIT Value	2800	YES		YES			Burst
1.2.17	30%-85% Post-EoT Rise Time (TRETOT)	2700	YES		YES			Burst	

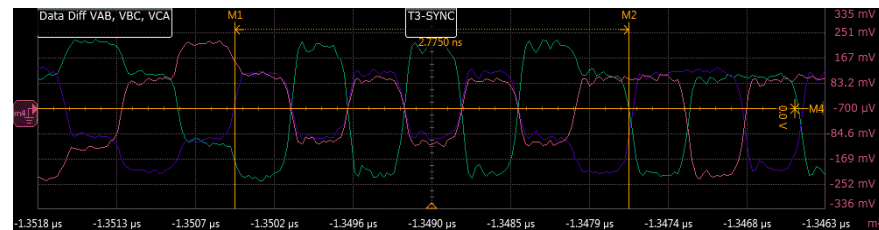
Enabled Protocol Related Test item



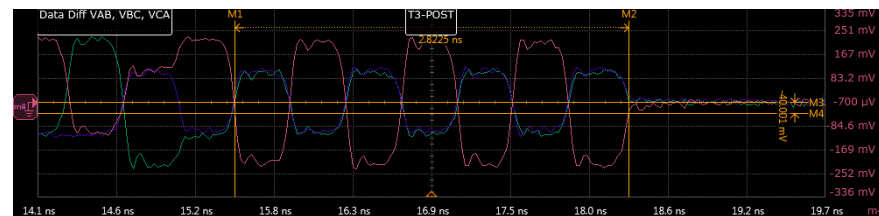
T3-PREBEGIN



T3-PREEND



T3-SYNC



T3-POST

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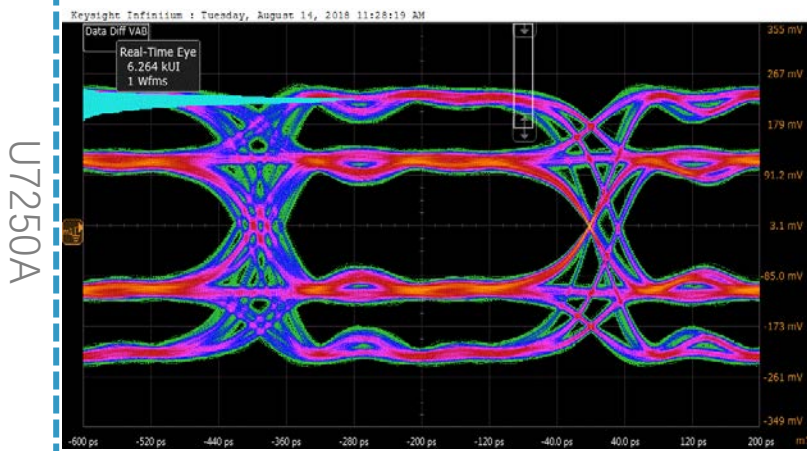
# Keysight U7250A C-PHY Tx test software

## Test result example

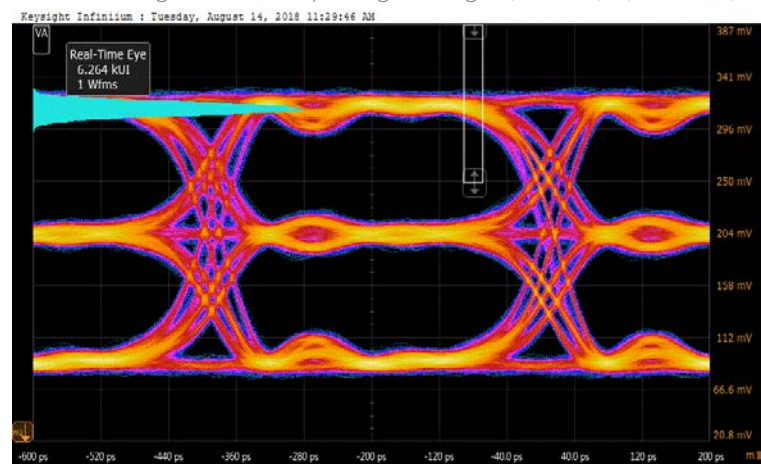
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1.2.7 HS-TX Differential Voltages (VOD-AB, VOD-BC, VOD-CA)



1.2.9 HS-TX Single-Ended Output High Voltages (VOHHS(VA), VOHHS(VB), VOHHS(VC))



CTS simulation

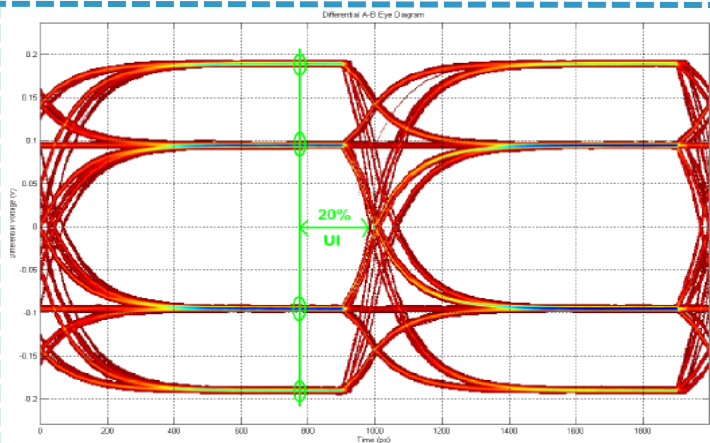
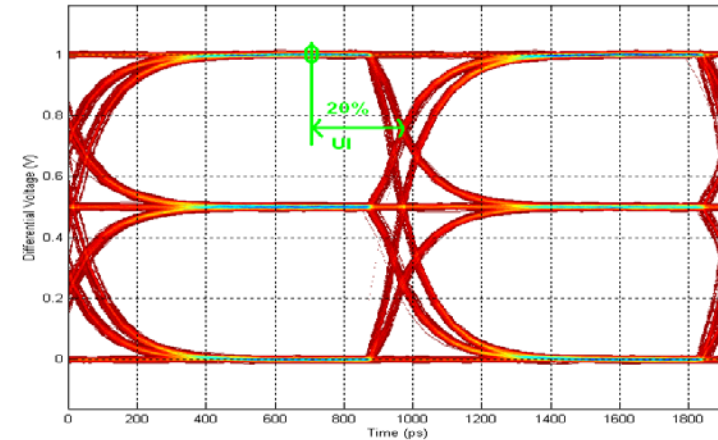


Figure 1.2.7-3: Sample  $V_{OD}$  Measurement at 20% UI Width

HS Eye Diagram



# Keysight U7250A C-PHY Tx test software

## Clock recovery

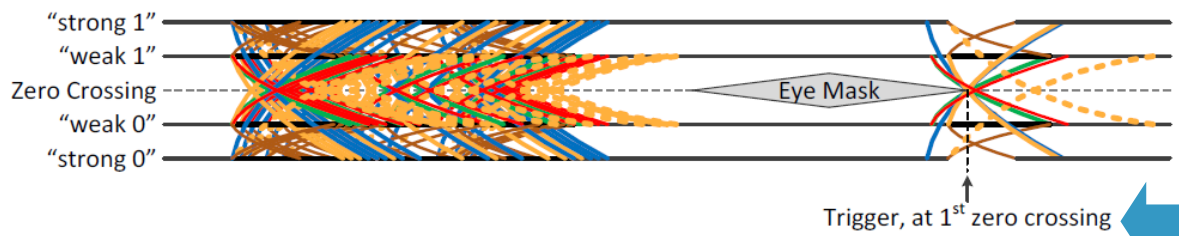


Figure 63 C-PHY Eye Pattern Example, Triggered Eye

Clock is recovered from the earliest edge of a symbol transition.



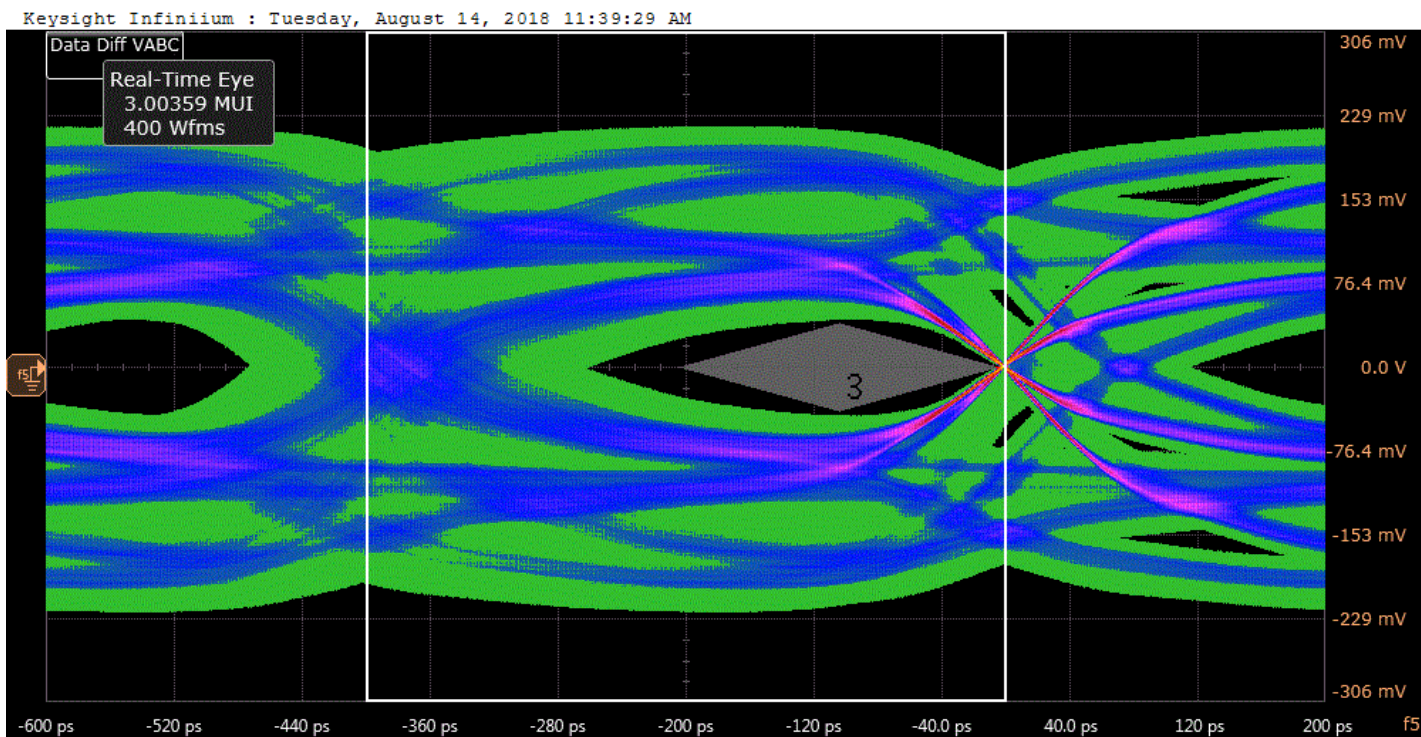
- 2. Using function make VAB, VAC, VBC (Symbol transition)
- 3. Among VAB, VAC, VBC, find each first arrival edge on acquired signal and build clock recovery
- 1. Acquire VA, VB, VC at once

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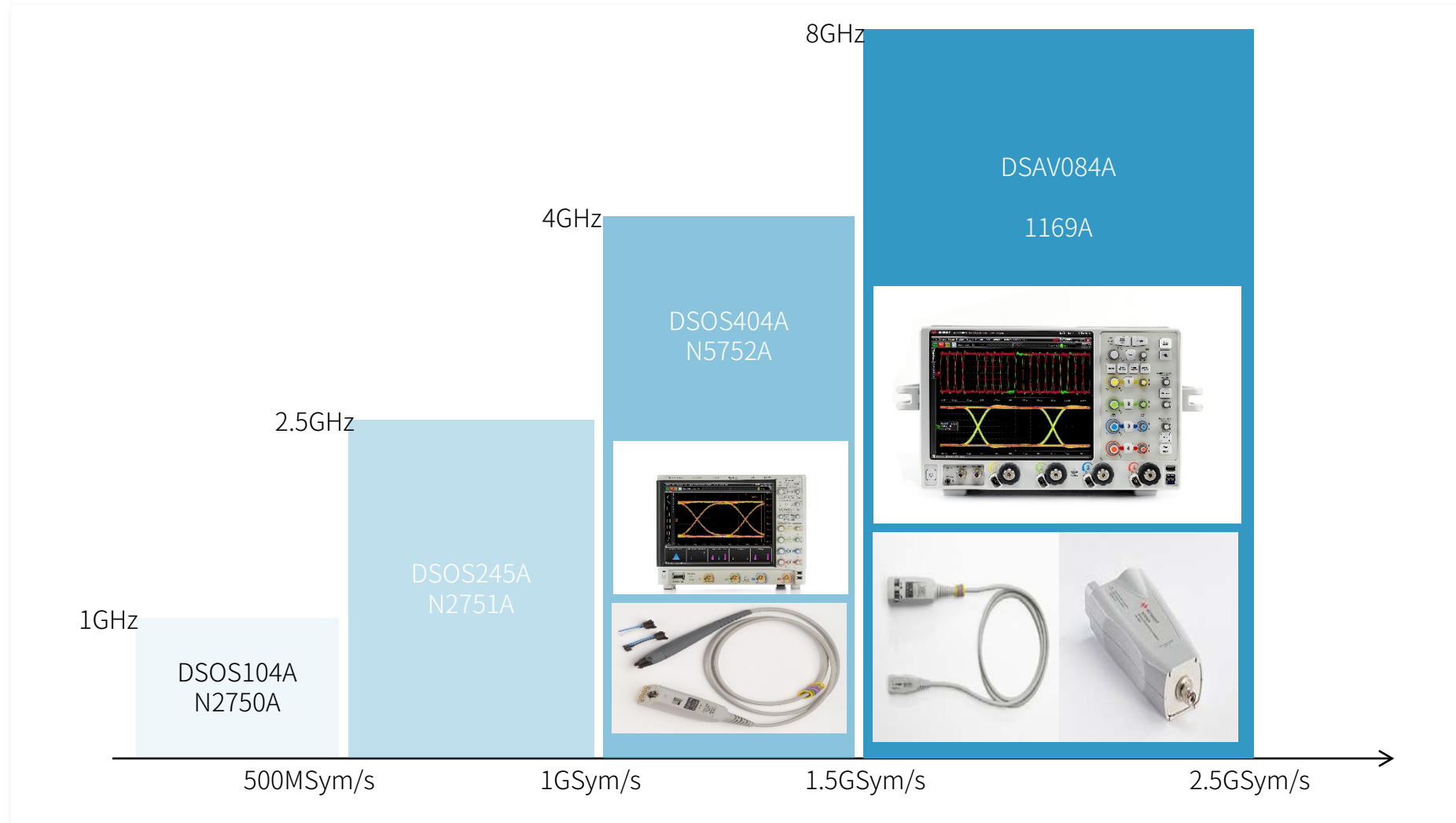
# Keysight U7250A C-PHY Tx test software

## Eye diagram Test result example



Test 1.2.21 Eye diagram test  
example with Standard  
channel embedding

# Keysight Solutions for MIPI TX PHY-test



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# MIPI TX Test Solutions

## Product Number

	<500MSym/s	<1GSym/s	<1.5GSym/s	≤ 2.5GSym/s
Oscilloscope	DSOS104A	DSOS254A	DSOS404A	DSAV804A
Probe	N2750A: 1.5GHz active probe x3	N2751A: 3.5GHz active probe x3	N2752A: 6GHz active probe x3	1169A: 12GHz active probe x3 And N7010A: active termination adapter x3
Software	U7250A: MIPI C-PHY conformance test application E2688A: Serial data analysis/mask testing with clock recovery N5414B: InfiniiScan software N5465B: InfiniiSim waveform transformation toolset			

Oscilloscope base line software must be same or above 6.20

# Agenda

Transmitter Testing

Receiver Testing

# About Receiver (RX) testing

## RX testing

An RX test is used to determine an RX' s capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing...

- A Bit Error Ratio Tester' s (BERT) Pattern Generator (BERT PG) is used to emulate a system' s TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.  
This signal has to be calibrated according to the specification
- The input of the RX under test is stimulated with this signal
- Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

# Jitter Tolerance Calibration and Measurement

- Calibrate the Rise/Fall times from the test equipment generator to approx. 115ps using 20%-80% transition time converter
- Calibrate the Eye width of three differential signals A-B, B-C, A-C to be 0.7UI by adding Jitter (e.g. DCD) over the already present switching jitter, of course using proper C-PHY clock recovery algorithm.
- Add ISI jitter by either using a HW channel or SW-programming of the generator to meet the 0.3UI of channel ISI requirement.
- Tune the Amplitude and the amount of ISI to meet the eye mask requirement of +40 to -40mV for EH and 0.4UI for EW.  
(Allow 10% of variation in calibration over the time scale wrt. the targeted eye mask spec.)
- After generating the worst case eye as per the mask requirements, Check for any errors in the receiver by comparing the received pattern with the receiver expected pattern and varying DC Common mode.



# How to Test MIPI C- /D-PHY RXs acc. to CTS?

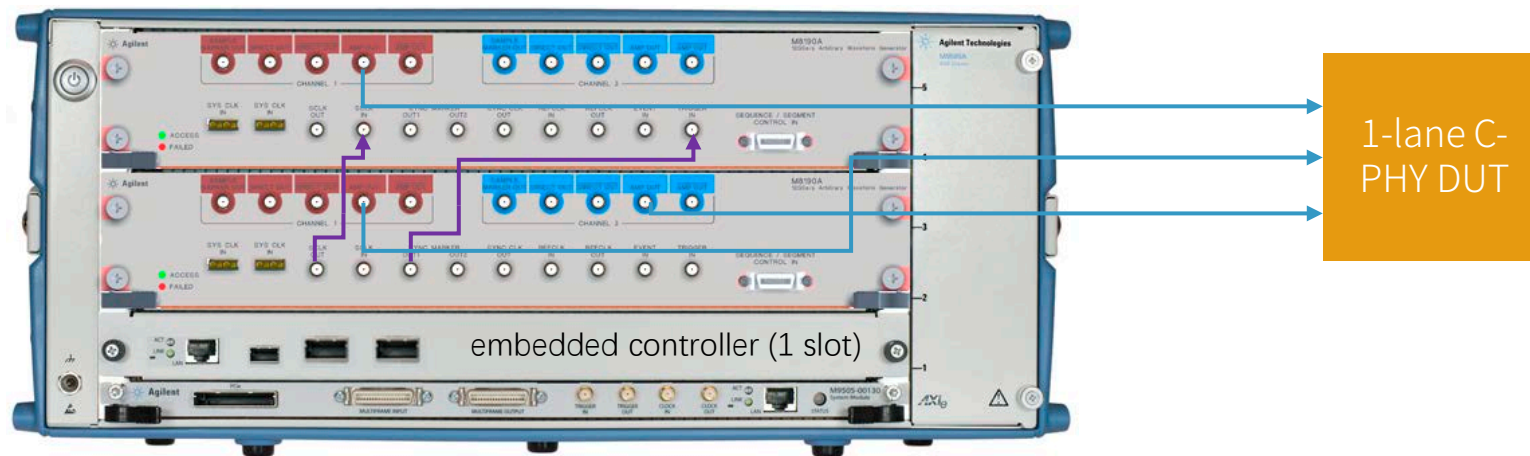
## Keysight M8000 Series of BER Test Solutions!

- Modular system in AXI form factor consisting of
  - AWG modules M8190/95A  
(used for multilevel and non-NRZ signals)
  - BERT modules M8041A and M8051A  
(used for two level, NRZ (and similar) signals)
  - plus M8070A SW with application plug ins (e.g. M8085 for MIPI)
  - Keysight J-BERT M8020A (=M8041/51A +M8070A SW)
    - modular up to 4 channels  
enabling channel skew measurements
    - Very well suited for M-PHY
    - Very much comparable to N4903
- Test Automation SW: Keysight N5990A
  - option 165 & 365 for MIPI M-PHY  
using w/ J-BERT M8020A or N4903B



# Setup for C-PHY, single lane:

M8190A, 5 Slot Frame, Embedded Controller



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# Setup for C-PHY, single lane:

M8195A, 5 Slot Frame, Embedded Controller



4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)

# Setup for C-PHY, single lane:

M8195A, 5 Slot Frame, Embedded Controller



4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)

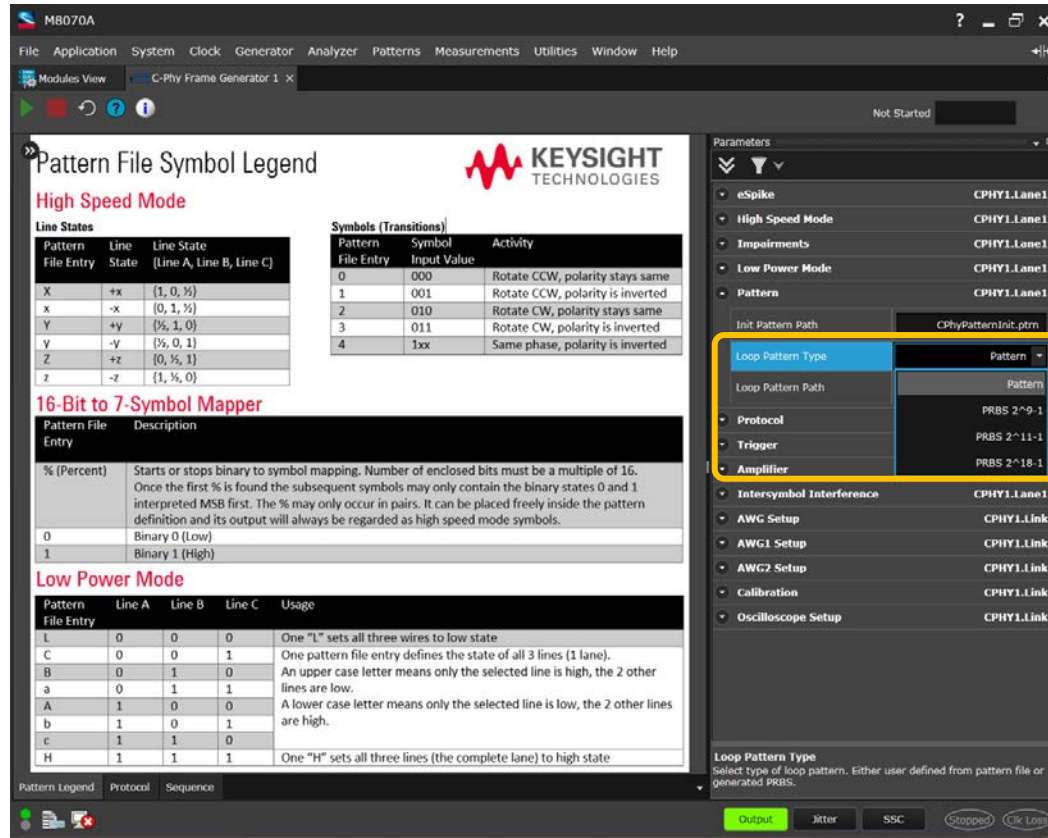
Alternative setup: M8195A, 2 slot frame, embedded Controller





# Realization of "C-PHY-editor" within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW



HS-Pattern can be set up as

- Serial data (encoder is integrated)
- Symbol value (0,1,2,3,4)
- Wire state (+/- x,y,z)
- Predefined PRBS

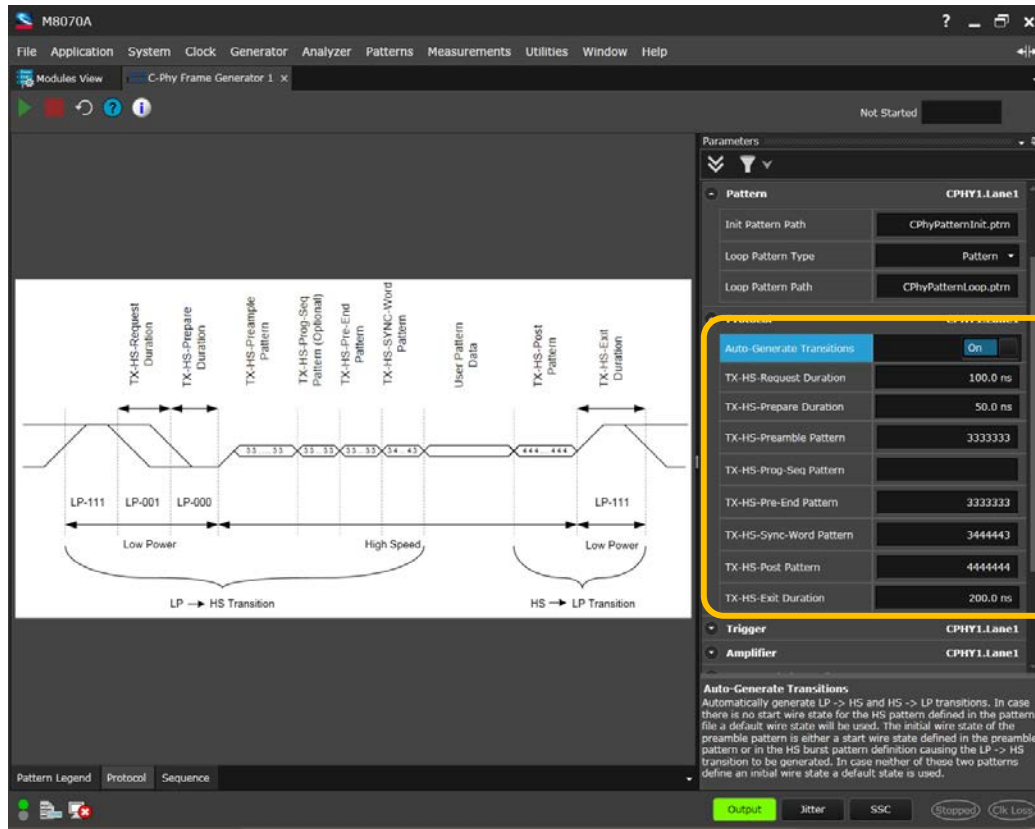
LS-Pattern

(8 possible states)

- can be set up as symbols (L, H, a, A, b, B, c, C)

# Realization of "C-PHY-editor" within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW



Set up of a sequence with LP - HS patterns, transition generated automatically

Parameters and patterns can be edited

# Realization of "C-PHY-editor" within M8000

M8085A option CT1 / CN1 as a Plug-In for the M8070A SW

The screenshot displays the M8070A software interface. The main window is titled "M8070A" and contains several panels. On the left, the "Pattern File Symbol Legend" panel is visible, which includes sections for "High Speed Mode" and "Low Power Mode". The "High Speed Mode" section contains two tables: "Line States" and "Symbols (Transitions)". The "Low Power Mode" section contains a table for "16-Bit to 7-Symbol Mapper". On the right, the "Parameters" panel is open, showing settings for "CPHY1.Lane1". This panel includes sections for "Impairments", "Low Power Mode", "Pattern", "Protocol", "Trigger", "Amplifier", and "Intersymbol Interference". The "Impairments" section is highlighted with a yellow box, and the "Intersymbol Interference" section is also highlighted with a yellow box. The "Intersymbol Interference" section includes an "Enabled" checkbox (set to "Off") and three "S-Parameter File" entries (A, B, and C), each with a corresponding ".s2p" file path.

Line States		
Pattern File Entry	Line State	Line State {Line A, Line B, Line C}
X	+x	{1, 0, ½}
x	-x	{0, 1, ½}
Y	+y	{½, 1, 0}
y	-y	{½, 0, 1}
Z	+z	{0, ½, 1}
z	-z	{1, ½, 0}

Symbols (Transitions)		
Pattern File Entry	Symbol Input Value	Activity
0	000	Rotate CCW, polarity stays same
1	001	Rotate CCW, polarity is inverted
2	010	Rotate CW, polarity stays same
3	011	Rotate CW, polarity is inverted
4	1xx	Same phase, polarity is inverted

16-Bit to 7-Symbol Mapper				
Pattern File Entry	Line A	Line B	Line C	Usage
L	0	0	0	One "L" sets all three wires to low state
C	0	0	1	One pattern file entry defines the state of all 3 lines (1 lane).
B	0	1	0	An upper case letter means only the selected line is high, the 2 other lines are low.
a	0	1	1	A lower case letter means only the selected line is low, the 2 other lines are high.
A	1	0	0	
b	1	0	1	
c	1	1	0	
H	1	1	1	One "H" sets all three lines (the complete lane) to high state

Parameters	
Impairments	CPHY1.Lane1
High Speed Rise Time	200 ps
High Speed Fall Time	200 ps
Sinusoidal Jitter Amplitude...	0 ps
Sinusoidal Jitter Frequency	100.00 MHz
Bounded Uncorrelated Jitte...	0 ps
Analog Skew A	0 ps
Analog Skew B	0 ps
Analog Skew C	0 ps
Low Power Mode	CPHY1.Lane1
Pattern	CPHY1.Lane1
Protocol	CPHY1.Lane1
Trigger	CPHY1.Lane1
Amplifier	CPHY1.Lane1
Intersymbol Interference	CPHY1.Lane1
Enabled	<input type="checkbox"/> Off
S-Parameter File A	SParameterFileA.s2p
S-Parameter File B	SParameterFileB.s2p
S-Parameter File C	SParameterFileC.s2p

Set-up of parameters in a BERT-like fashion

HS-impairments

ISI via S-parameters

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# GUI for C-PHY CTS Calibration and Test Procedures

The screenshot displays the MIPI C-PHY Editor GUI for CTS calibration and testing. The interface is divided into several sections:

- Measurement History:** Shows a diagram of the test setup with two modules (1st and 2nd) connected to an AWG and an oscilloscope. Below the diagram, it states: "Test set-up / cabling".
- Results Table:** A table showing the results of calibration or measurement steps. The columns are "Result", "Set Level [mV]", and "Measured Level [mV]".
- Graph:** A line graph showing the relationship between "Set Level [mV]" (x-axis) and "Measured Level [mV]" (y-axis). The data points form a straight line, indicating a linear relationship. A yellow annotation reads: "graphical representation of calibration or measurement".
- Parameters:** A panel on the right side of the graph showing configuration parameters for "LP Level Calibration High Data0 A .System".
- Event Logging:** A bottom section showing a log of events, including calibration steps and the final test result.

Result	Set Level [mV]	Measured Level [mV]
pass	1300	1185
pass	1250	1138
pass	1200	1090
pass	1150	1043
pass	1100	995
pass	1050	948
pass	1000	900
pass	950	853
pass	900	805
pass	850	758
pass	800	710
pass	750	663
pass	700	615
pass	650	567
pass	600	520

Parameters for LP Level Calibration High Data0 A .System:

- Max LP High Level: 1.3 V
- Min LP High Level: 600 mV
- Offline: Off
- Step Size: 50 mV
- Transfer Function Ch...: DoNothing.tf2
- Transfer Function Ch...: DoNothing.tf2
- Use Infnisim: Off

Event Logging:

- Step 13 - Calibrating V<sub>OH</sub> = 650 mV; V<sub>OL</sub> = 0 V
- Step 14 - Calibrating V<sub>OH</sub> = 600 mV; V<sub>OL</sub> = 0 V
- Test Passed Offline

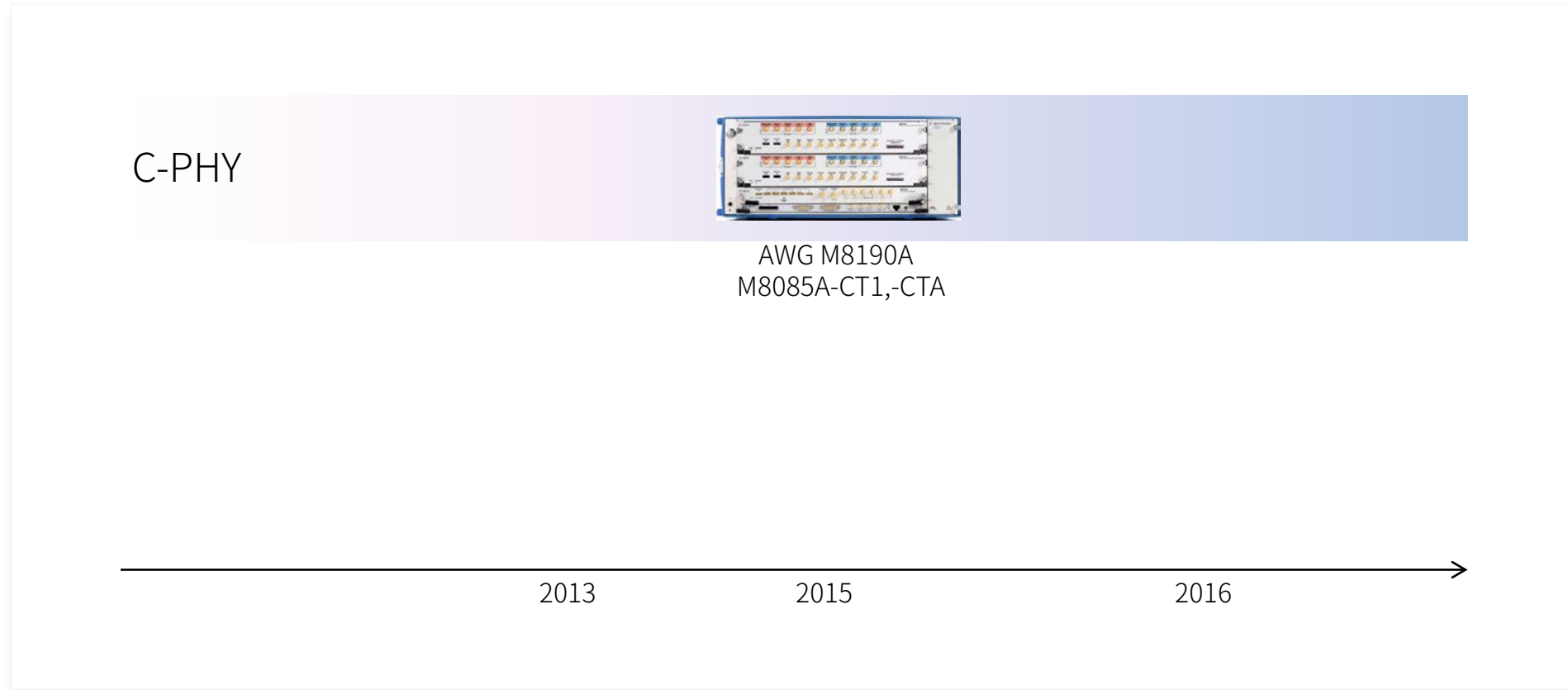
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# Keysight Solutions for MIPI RX PHY-test

2015: M8085A w/ M8190A addressing C-PHY

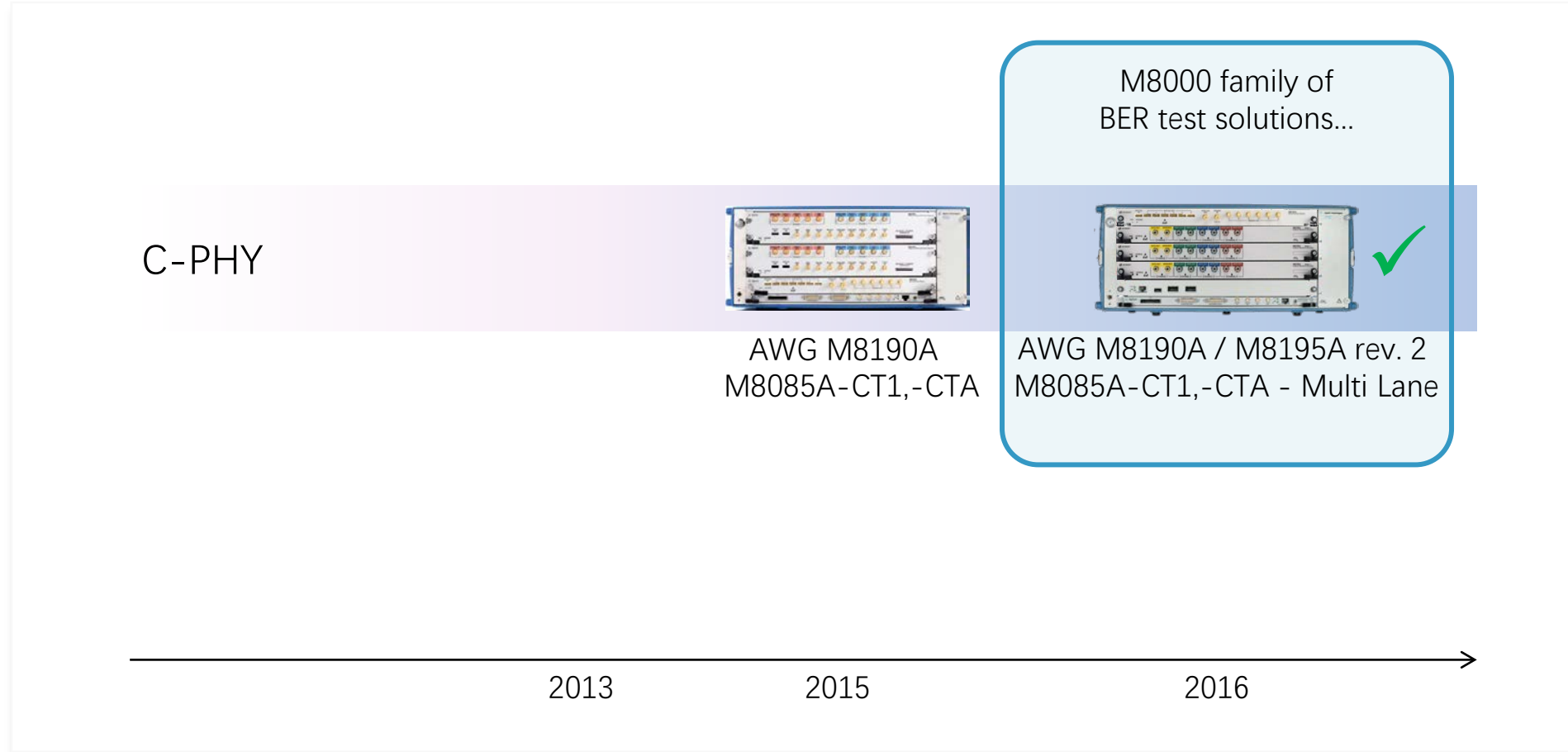


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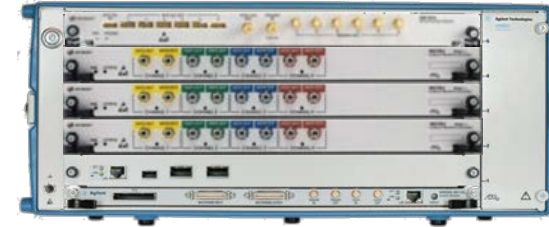
# Keysight Solutions for MIPI RX PHY-test

2016 and beyond: M8085A w/ M8195A rev. 2



# MIPI RX Test Solutions

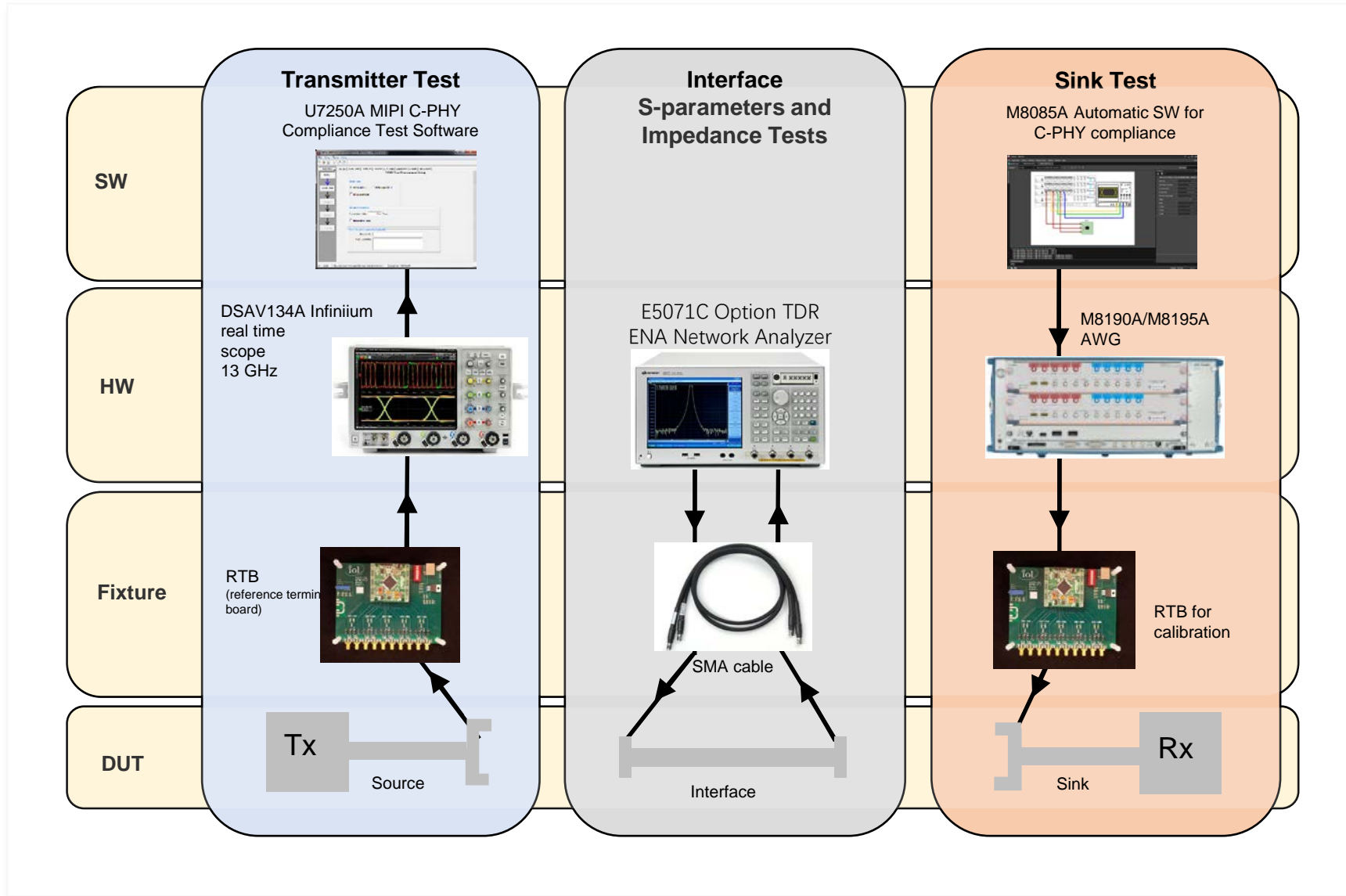
Availability and Product / Option Number



	M8085A	
Instrument / HW	M8190A	M8195A, rev. 2
Link-type	Single-lane	Multi-lane
C-PHY	N5990A-010, CT1, CTA Sept. 2015	N5990A-010, CT1, CTA Q2FY2016

M8070A rev 3.0 or higher is required to host the M8085A PlugIns  
All "T" licenses also available as "N" = network license

# Keysight MIPI C-PHY Solution Coverage



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# THANKS



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