

# USB 3.1 Gen2 10G - Gen1 5G Receiver Testing with J- BERT M8020A

# Agenda

USB 3.1 gen1 vs. gen2 overview

LFPS

Repeater / Re-Drivers / Re-Timers

128b/132b

SKPOS

Jitter Tolerance

USB 3.0 ECN 015 and ECN 018

N5990A Test Automation SW

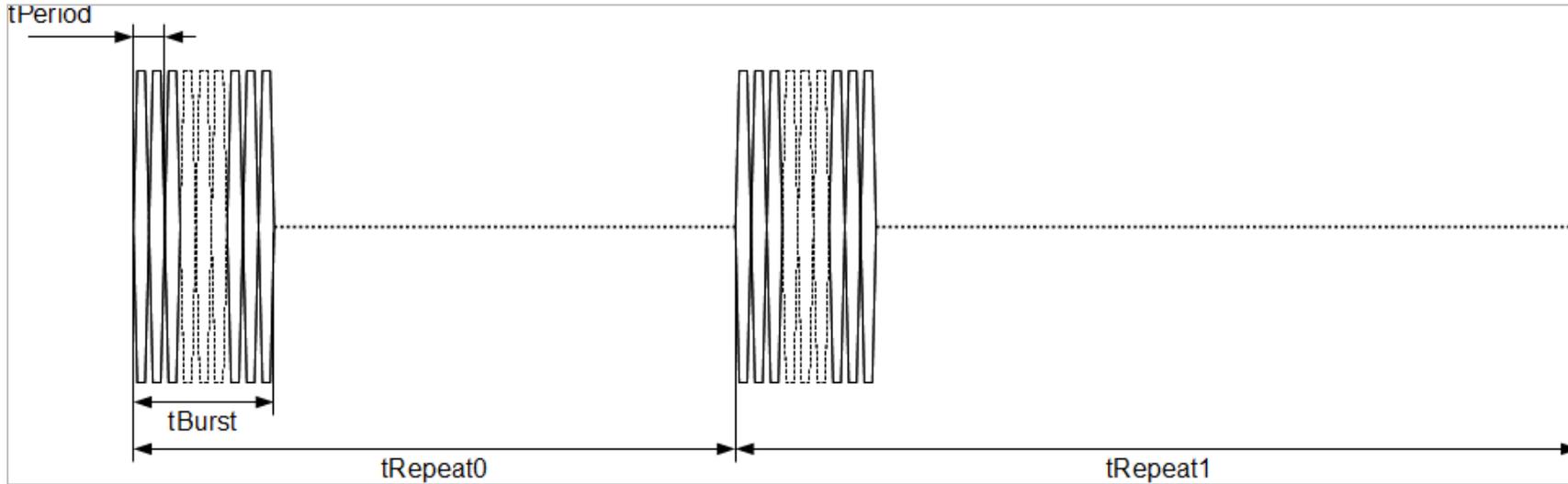
Channel Add Setup for HighSpeed and LFPS Testing

RX Test Setup

# USB 3.1 Gen 1 vs. Gen 2 Overview

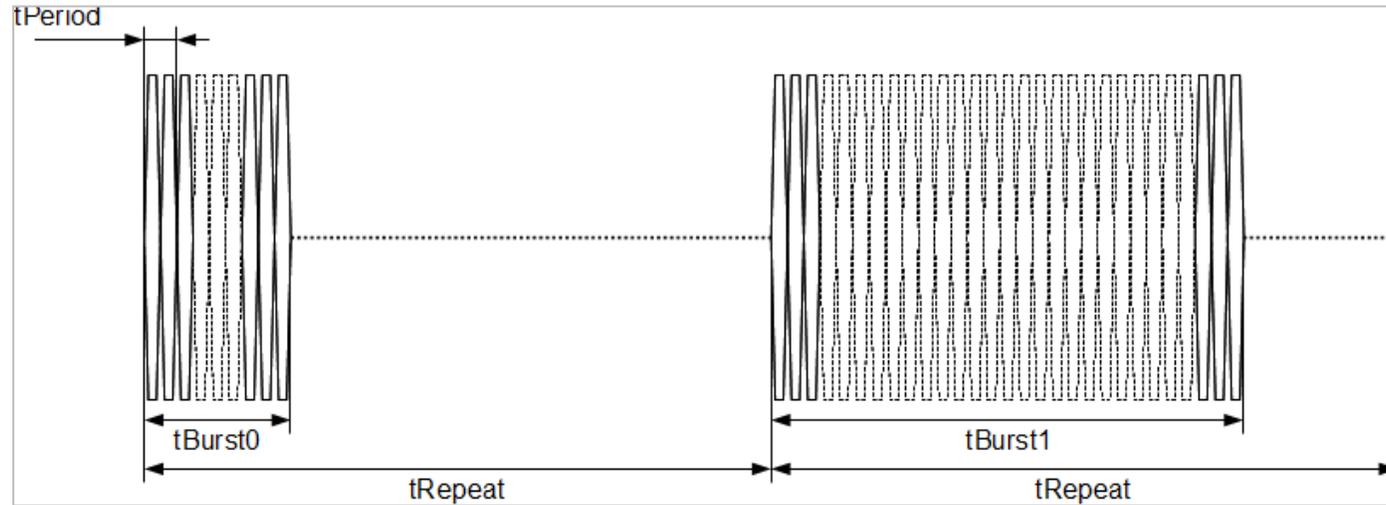
	Gen 1	Gen 2
Data rate	5Gb/s $\pm$ 300ppm (SSC variations not accounted for)	10Gb/s $\pm$ 300ppm (SSC variations not accounted for)
Coding	<ul style="list-style-type: none"> <li>- 8b/10b</li> <li>- scrambler: <math>G(X) = X^{16} + X^5 + X^4 + X^3 + 1</math></li> <li>- scrambler reset by COM (K28.5) or BRST</li> <li>- seed: FFFFh</li> <li>- Symbol lock: K28.5, some implementations might be able to use K28.1 or K28.7</li> </ul>	<ul style="list-style-type: none"> <li>- 128b/132b</li> <li>- scrambler: <math>G(X) = X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1</math></li> <li>- scrambler reset by SYNC OS</li> <li>- seed: 1D BFBCh</li> <li>- Block alignment: SYNC OS + SDS OS and realignment through SKP OS</li> </ul>
SKP	K28.1, K28.1	SKPOS with variable number of SKPs
LFPS		Device host capability negotiation is done during LFPS phase using LFPS modulation schemes
CDR	PLL transfer: <ul style="list-style-type: none"> <li>- <math>f_{3dB} = 10\text{MHz}</math></li> <li>- <math>\text{peaking}_{\text{max}} = 2\text{dB}</math></li> </ul> HPF transfer: <ul style="list-style-type: none"> <li>- <math>f_{3dB} = 4.9\text{MHz}</math></li> <li>- <math>\text{peaking} \approx 0\text{dB}</math></li> <li>- <math>\text{damping factor} = 0.707</math></li> </ul>	PLL transfer: <ul style="list-style-type: none"> <li>- <math>f_{3dB} = 15\text{MHz}</math></li> <li>- <math>\text{peaking}_{\text{max}} = 2\text{dB}</math></li> </ul> HPF transfer: <ul style="list-style-type: none"> <li>- <math>f_{3dB} = 7.5\text{MHz}</math></li> <li>- <math>\text{peaking} \approx 0\text{dB}</math></li> <li>- <math>\text{damping factor} = 0.707</math></li> </ul>
SSC	<ul style="list-style-type: none"> <li>- Modulation rate: 30kHz to 33kHz</li> <li>- Deviation: +0 to -4000(min)/-5000(max)</li> <li>- Max slew rate: 10ms/s</li> </ul>	<ul style="list-style-type: none"> <li>- Modulation rate: 30kHz to 33kHz</li> <li>- Deviation: +0 to -4000(min)/-5000(max)</li> <li>- New df/dt requirement: 1250 (max) ppm/<math>\mu</math>s instead of max slew rate spec</li> </ul>
De-emphasis	Post: -3dB	Pre: 2.7dB Post: -3.3dB

# LFPS – SCD1 & SCD2 – tRepeat Modulation



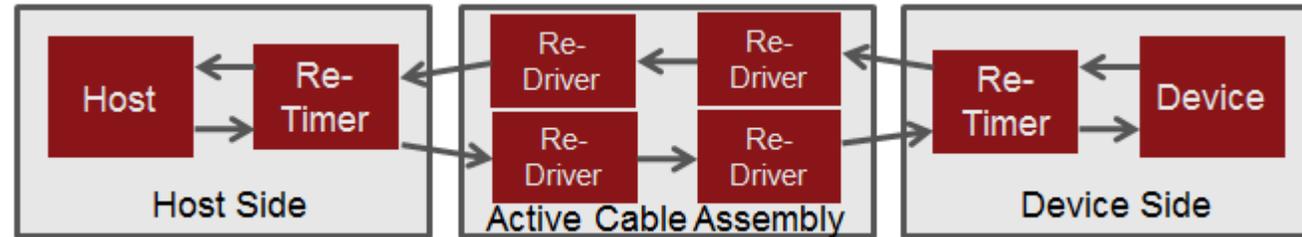
- $tRepeat$  is modulated to express 0 (short) and 1 (long)
- SCD1.LFPS (4' b0100), and SCD2.LFPS (4' b1101)
- SuperSpeed+ identity check

# LFPS – LBPM Encoding



- Rate (speed and lane) announcement and negotiation
- Repeater declaration
- Power state transition in repeater
- Can be expanded to:
  - VBus control on/off, overcurrent sensing
  - Power delivery
  - Vendor specific operation

# Repeater – Re-Driver – Re-Timer



- A link can contain multiple repeaters
- Repeater devices can be of different types
  - Re-timer
  - Re-driver
- Repeaters are declared in LBPM
- A maximum of 10 elastic buffers could be involved in loopback
  - more SKPOS required
  - send 5 SKPOS instead of 1 SKPOS every 22 blocks

# 128b/132b Coding

- 4 bit header to avoid link reset problems from PCIe 8G
- 0011 marks a data block and 1100 a command block
- Same scrambler polynomial as PCIe 8G:  
 $G(X) = X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$   
Block header bypasses scrambler and does not advance scrambler
- Command block scrambler rules
  - TS1, TS2, TSEQ
    - symbol 0 bypasses but advances scrambler
    - symbols 1 to 13 are scrambled
    - symbols 14 and 15 bypass scrambler but advance scrambler if used for DC balance otherwise they are scrambled
  - SKP OS bypasses scrambler and does not advance scrambler
  - SDS OS bypasses scrambler but advance scrambler
- All blocks are 132b long except SKPOS which can be shorter or longer

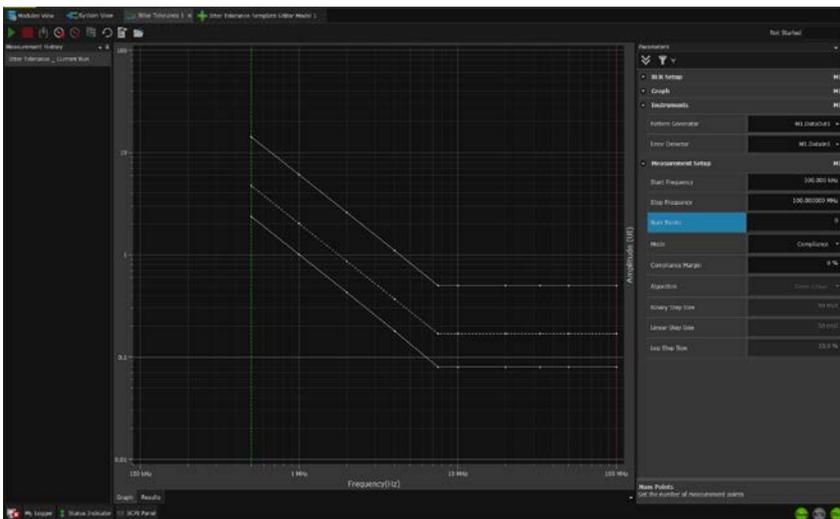
# SKPOS – gen2

- SKPOS:  $2n * SKPs + SKPEND$  symbol + 3 symbols for LTSSM state;  $n = 0$  to 18
  - SKP..CCh
  - SKPEND..33h
- SKPOS in average every 22 blocks
- ➔ The variable length of SKPOS is challenging for BERT EDs
- ➔ No BERT system currently on the market is able to deal with this
  
- Remark:
- SKPOS rules might change to
  - $4n * SKPs + SKPEND$  symbol + 3 symbols for LTSSM state;  $n = 1$  to 9
- This would ensure that every receiver in the link has at least 4 SKPs for clock compensation available

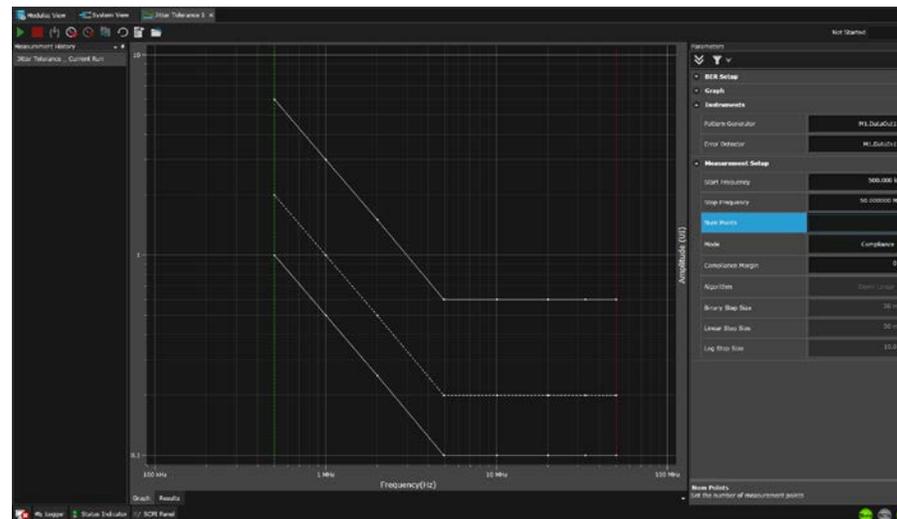
# Jitter Tolerance – Stress Components – Base Spec

	Gen1 5G	Gen2 10G
TJ after RX EQ	450mUI	394mUI
$RJ_{rms} / RJ_{pp \text{ ber}=1E-12}$	12.1mUI / 177.9mUI	13.08mUI / 192.3mUI
$SJ_{\text{out of CDR tracking range}}$	200mUI	170mUI
Channel	channel -20.6dB @ 5GHz → M8048A-001 12.8" + M8048A-002 14.4" is close. Shorter traces are available on the M8048A-001 to compensate for fixture and cable losses	

# Jitter Tolerance Settings – Base Spec

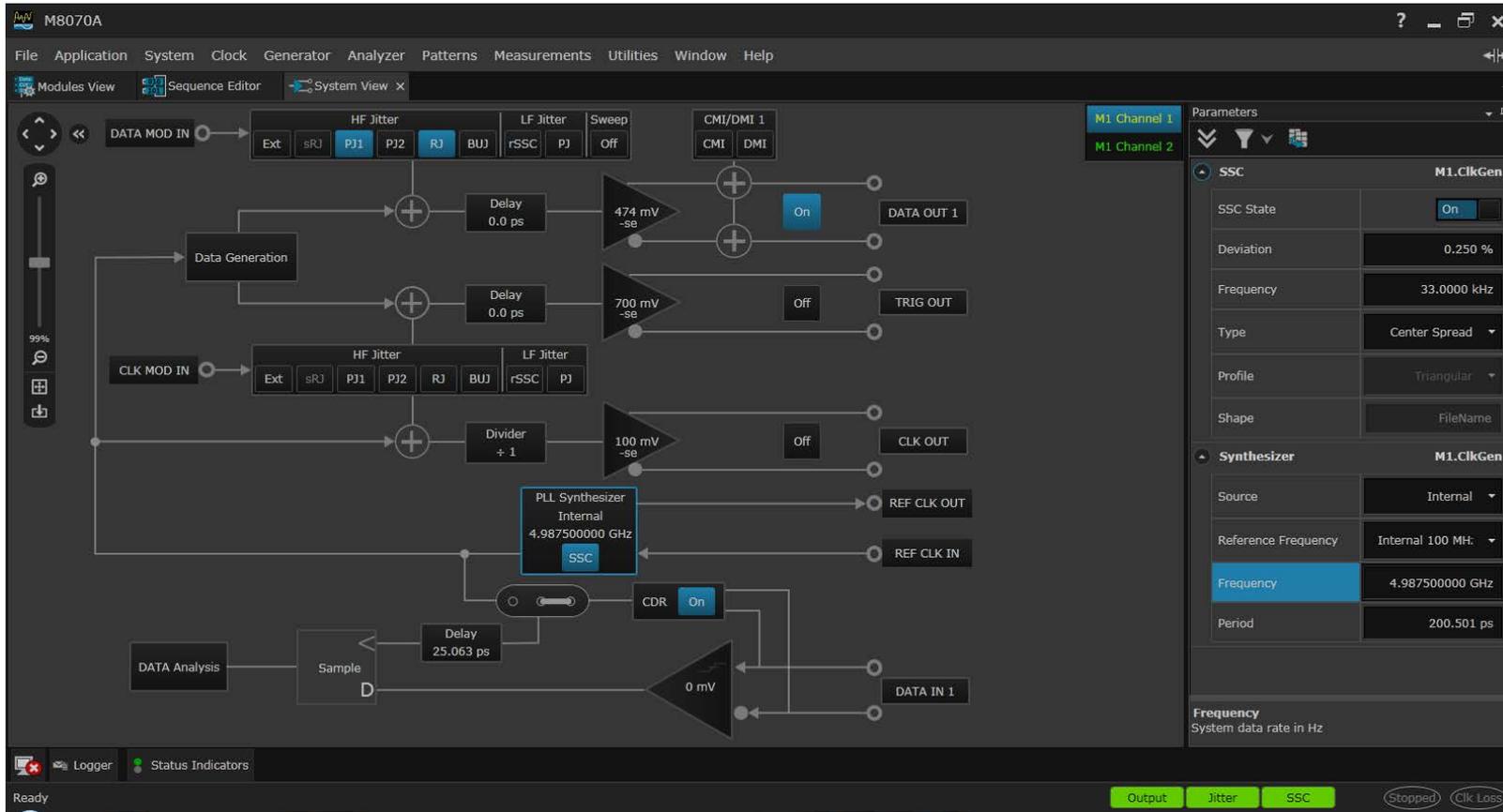


- Center Data Rate with SSC: 9.975Gb/s
- SSC: Center Spread 33kHz with 0.25%
- Voltage Swing @ TP1: 800mV
- Pre-shoot @ TP1: 2.7dB
- De-Emphasis @TP1: -3.3dB
- RJ: 1.308ps RMS



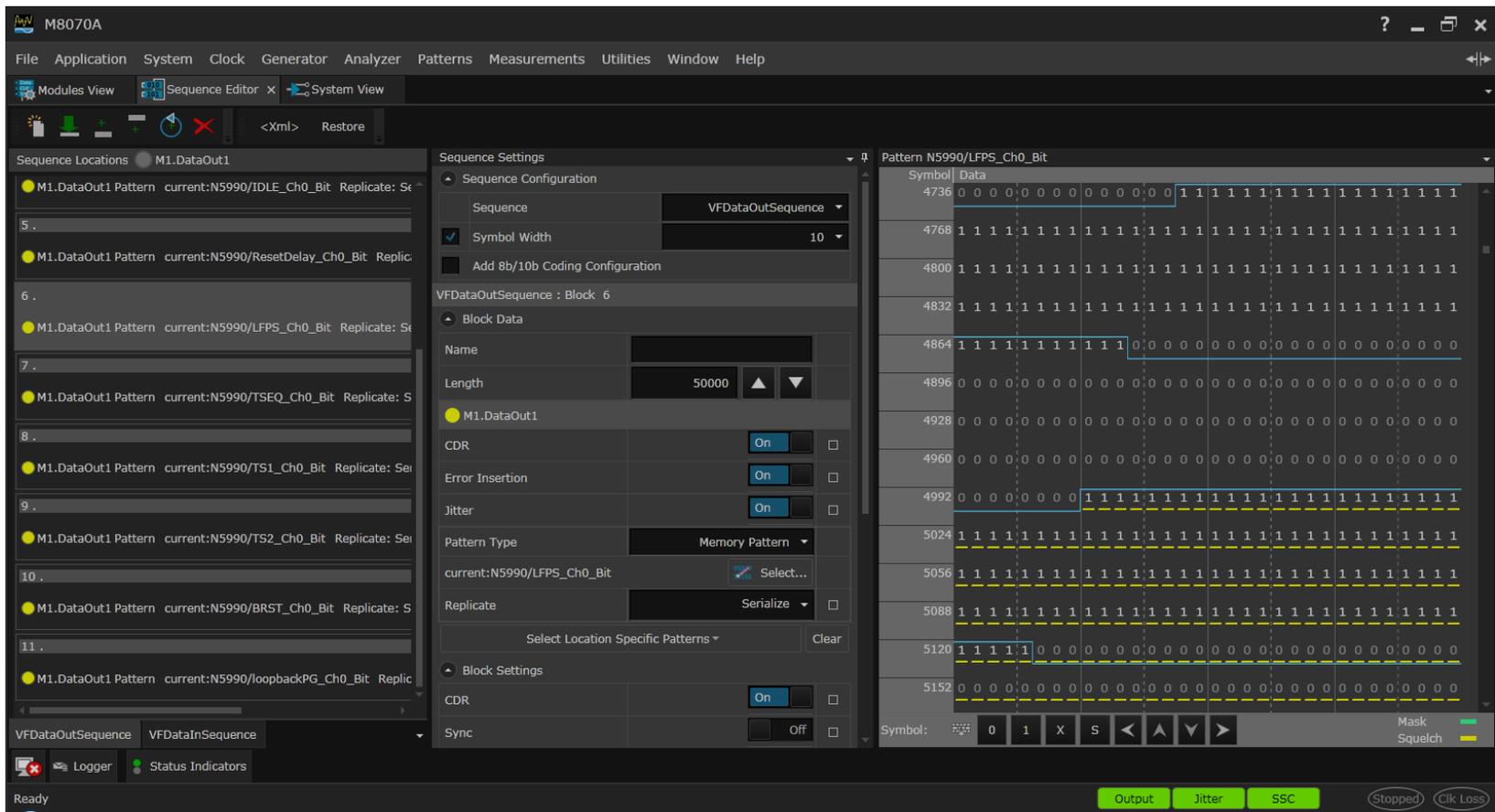
- Center Data Rate with SSC: 4.9875Gb/s
- SSC: Center Spread 33kHz with 0.25%
- Voltage Swing @ TP1: 750mV
- De-Emphasis @TP1: -3.0dB
- RJ: 2.42ps RMS

# System View



The System View provides a quick overview on stressor and output states

# Sequencer



Squelch is used on the outputs for a real electrical idle between LFPS bursts

# USB 3.0 – ECN 015 and ECN 018

## ECN 015:

- Changed minimum SSC spread from -0.4% to -0.2%
- New SSC spec:
  - +0% to min. -0.2% / max. -0.5%
- Compliance testing is done with 0.5% spread

## ECN 018:

- Allows a -0.2% offset on data rate to be more wireless friendly
- Limits SSC deviation for wireless friendly data rate
- New data rate and SSC spec for wireless friendly use case:
  - Data rate is 5Gb/s -0.2% → 4.99Gb/s +/- 300ppm
  - SSC for 4.99Gb/s is +0% to min -0.2% / max. -0.3%

# N5990A USB 3.0 Test Automation SW

The screenshot displays the N5990A Test Automation Software Platform interface. The main window is titled "N5990A Test Automation Software Platform" and features a menu bar (File, Station, Sequencer, Help) and a toolbar with icons for "Configure DUT", "Load", "Save", "Start", "Abort", "Pause", "Print", "Properties", and "Log List". A "Last 24 hours" filter is visible in the top right.

The left pane shows a tree view of test items under "USB3 - SuperSpeed Device". The "Loopback Training Optimization" item is selected and expanded, showing a list of sub-items with "NOT RUN" status. The right pane displays the configuration for "Loopback Training Optimization", including:

- Loopback Training Optimization**
  - Offline: False
- 1) Specification**
  - Eye Height: 145 mV
  - SSC: 5000 ppm
  - SSC Frequency: 33 kHz
- 2) Specification Margins**
  - Eye Height Margin: 2.5 mV
- Sequencer**
  - Procedure Error Case Behavior: Proceed With Next Procedure
  - Procedure Failed Case Behavior: Proceed With Next Procedure
  - Repetitions: 0

The bottom pane shows a log of events:

Severity	Message	Date
Progress	Instrument Connections	4/21/2014 3:57:08 PM
Progress	Opening online connection to M8020A J-BERT at M8070A	4/21/2014 3:57:08 PM
Progress	Opening offline connection to DSO Infinium Series at scope	4/21/2014 3:57:08 PM
Progress	Opening offline connection to U7243A at 192.168.0.104	4/21/2014 3:57:08 PM
Info	N5990A Test Automation Software Platform startup complete!	4/21/2014 3:57:09 PM
Info	Loopback Training Optimization started	4/21/2014 4:04:27 PM
Progress	Loopback Training Optimization: Step 0	4/21/2014 4:04:27 PM

The status bar at the bottom indicates "Performing procedure step 0 of iteration 0, total step count is 0" and "Running Online USB3 Station".

The "Loopback Training" dialog box is open on the right, showing the "Training Method" set to "WarmReset". The "Warm Reset" button is highlighted. The "Delay after Warm Reset(ms)" is set to 10. The "LFPS Idle" is set to "M8020A\_Idle". The "LFPS Polling" button is selected, with "Number of LFPS" set to 16. The "TSEQ" button is selected, with "Number of TSEQ" set to 65536. The "TS1" button is selected, with "Number of TS1s" set to 256. The "TS2" button is selected, with "Number of TS2s" set to 65536. The "BRST" and "Comma with SKP" buttons are also visible.

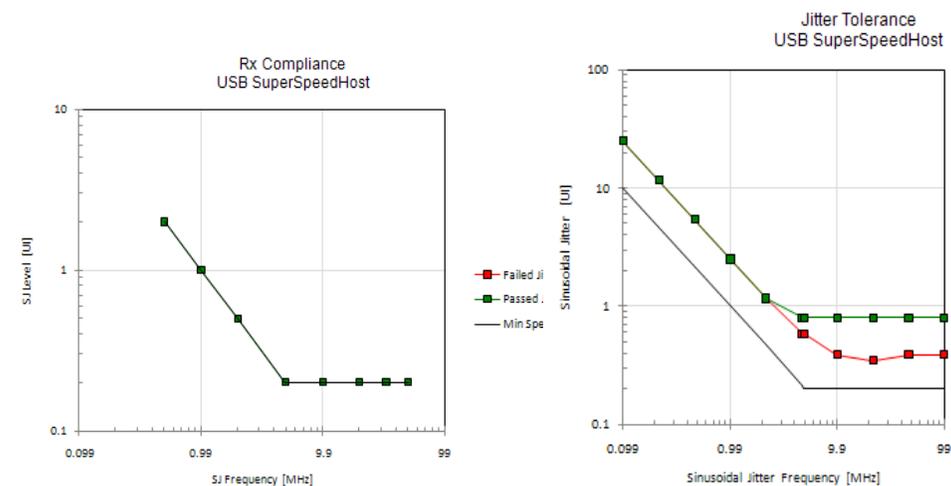
The "Voltage Settings" section is checked, with "Use Volt. Settings from Rx Tests" selected. The "J-BERT SER Detector" section shows "CDR Loop-Bandwidth" set to 6.00 MHz, "CDR Transition Density" set to 50.0 %, "CDR Peaking" set to 0.50 dB, and "Trigger Threshold" set to 100 mV. The "Polarity Inverted" checkbox is unchecked.

The "Status" is "Test not Running". The "Start", "Save parameters and Close", and "Close" buttons are visible at the bottom of the dialog.

# SuperSpeed Receiver Tests

## Rx Compliance and Jitter Tolerance Testing

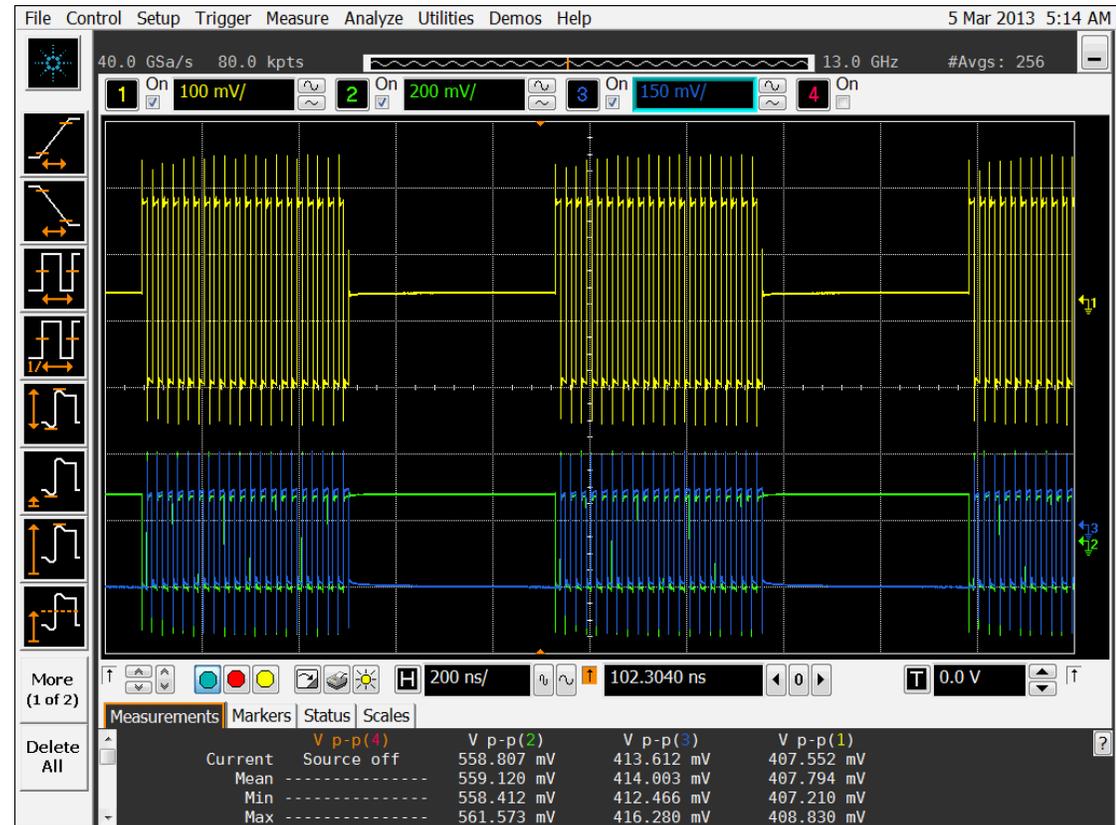
- Automated instrument control for:
  - Setup calibration
  - Compliance test
  - Characterization test
  - Support for debugging
- Operator guidance
- Sophisticated test reports
- Controls J-BERT, Oscilloscope.
- Supports full product characterization including transmitter measurements



Result	SJ Frequency [MHz]	Failed Jitter [UI]	Passed Jitter [UI]	Min Spec [UI]	Symbol Errors
pass	0.500		2.00	2.000	0
pass	1.000		1.00	1.000	0
pass	2.000		0.50	0.500	0
pass	4.900		0.20	0.200	0
pass	10.000		0.20	0.200	0
pass	20.000		0.20	0.200	0
pass	33.000		0.20	0.200	0
pass	50.000		0.20	0.200	0

# Channel Add – LFPS Tests and USB 2.0 RX Tests

- A channel add allows to create real electrical idle signaling with very fast transitions from data swing to 0 and vice versa
- Channel add can be used to
  - Test and characterize LFPS timing
  - Test and characterize USB 2.0 receivers



# Instrument Setup for RX Testing

## Expected RX Test Setup Without Accessories:

J-BERT M8020A with following options:

- C16 – 16G BERT (C08 – 8.5G BERT would be sufficient for USB 3.x 5G)
- 0G4 – De-emphasis
- 0G3 – Jitter Injection
- 0S1 – Clock Compensation for Error Detector (USB 3.x 5G supported with initial release; support for USB 3.1 10G is scheduled for late summer 2014)

## Useful Additional Options:

- 0G2 – Second Pattern Generator for USB 2.0 Tests and USB 3.x LFPS Tests
- 0A3 – Error Detector CTLE

## Control and Automation SW:

- M8070A – 0TP or M8070A – 0NP – M8020A System SW
- N5990A – 010 + N5990 – 102 USB 3.0 RX Test Automation
- TBD – USB 3.x Link Training Suite

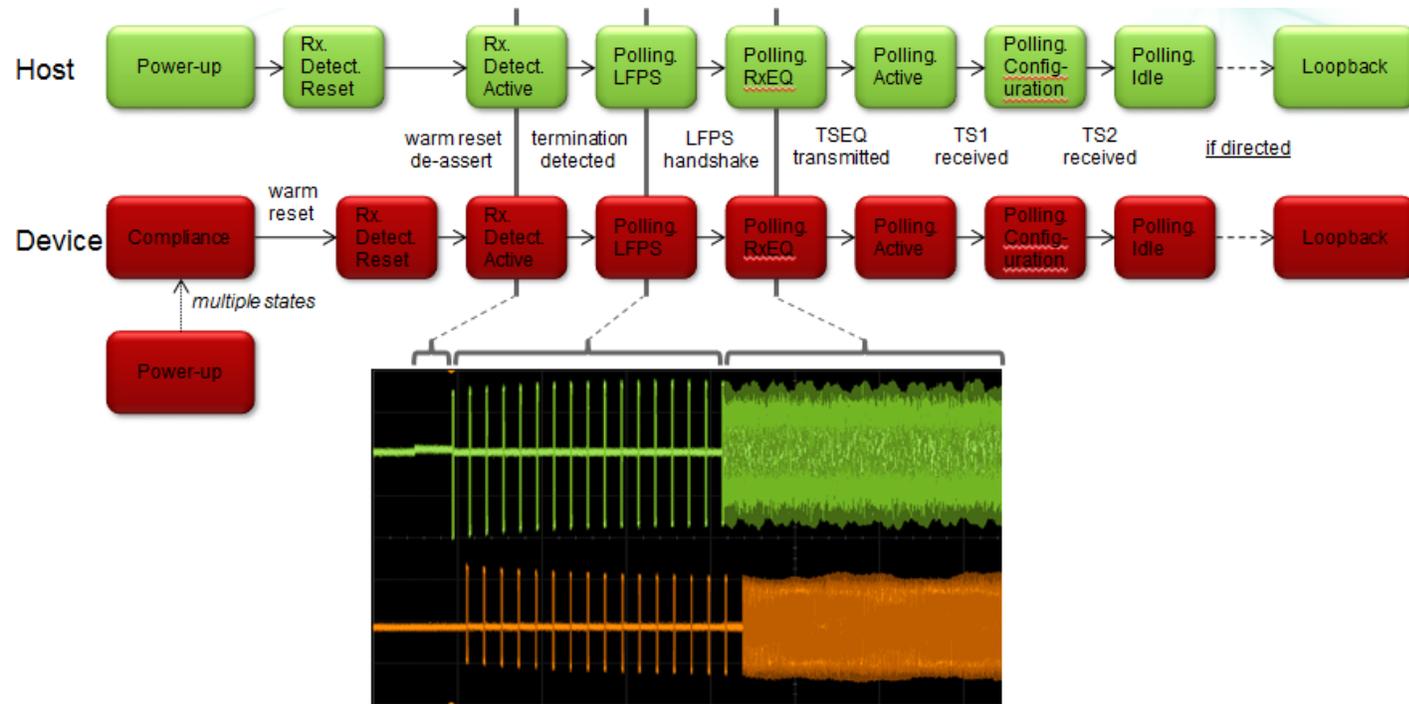
## Mainframe:

- M8020A – BU2 – 5-slot AXIe chassis with USB option

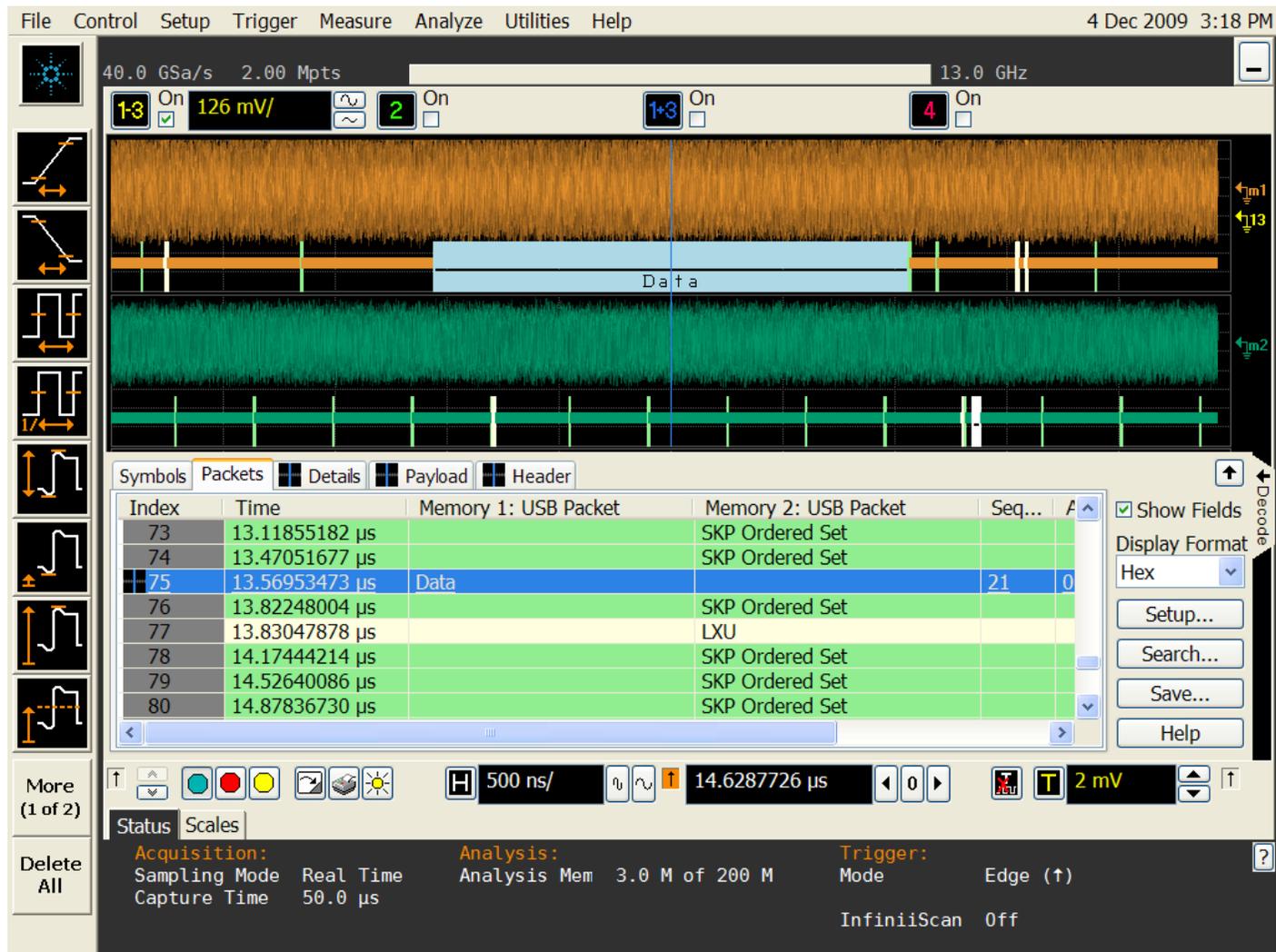
# Typical SuperSpeed Link

## Turn-on Sequence

### LTSSM states:

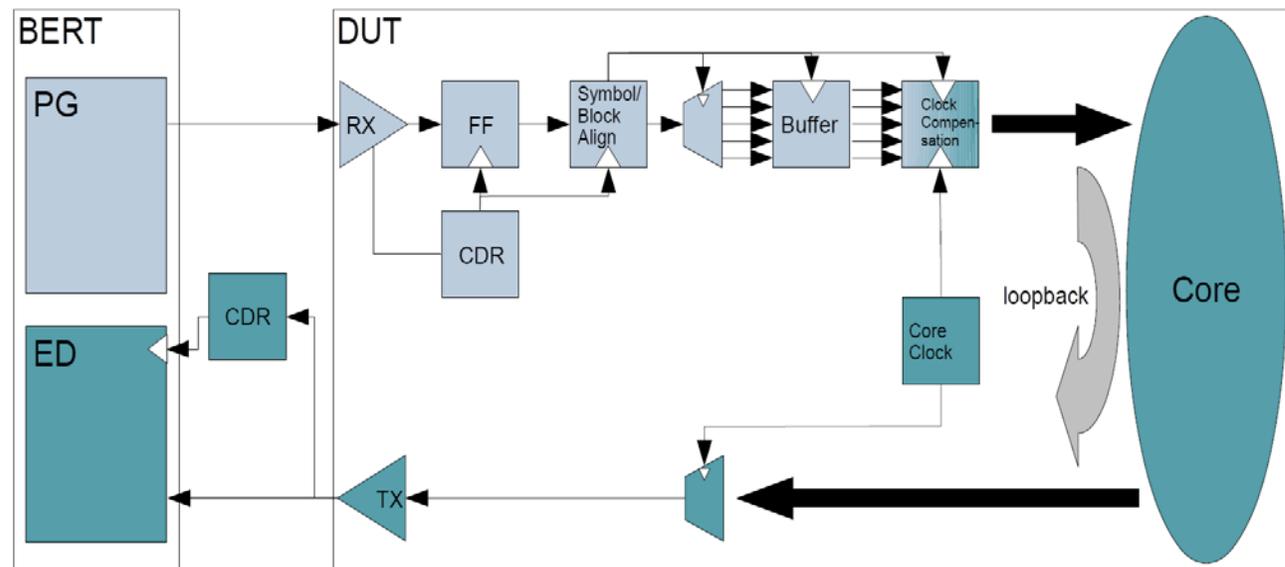


- J-BERT' s sequence trigger can be used to trigger scope captures for each training step → in combination with scope' s protocol decode very helpful for debugging a training sequence



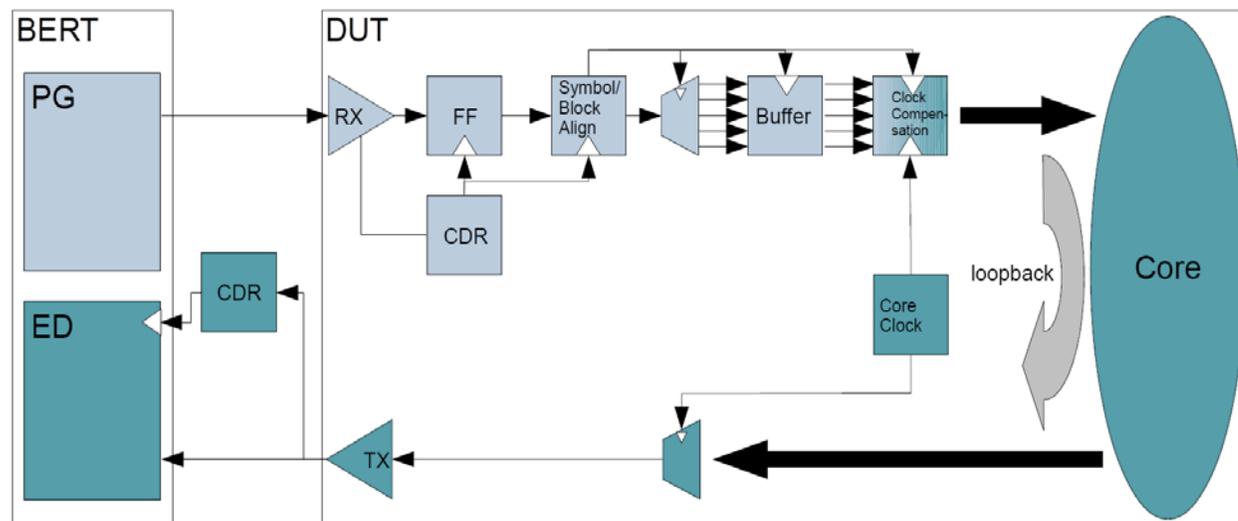
# Loopback – 1

- BERT and DUT run in separate clock domains
- DUT has to modify SKPOS for clock compensation
- Test pattern is modified → normal BER comparison does no longer work
- What to do?

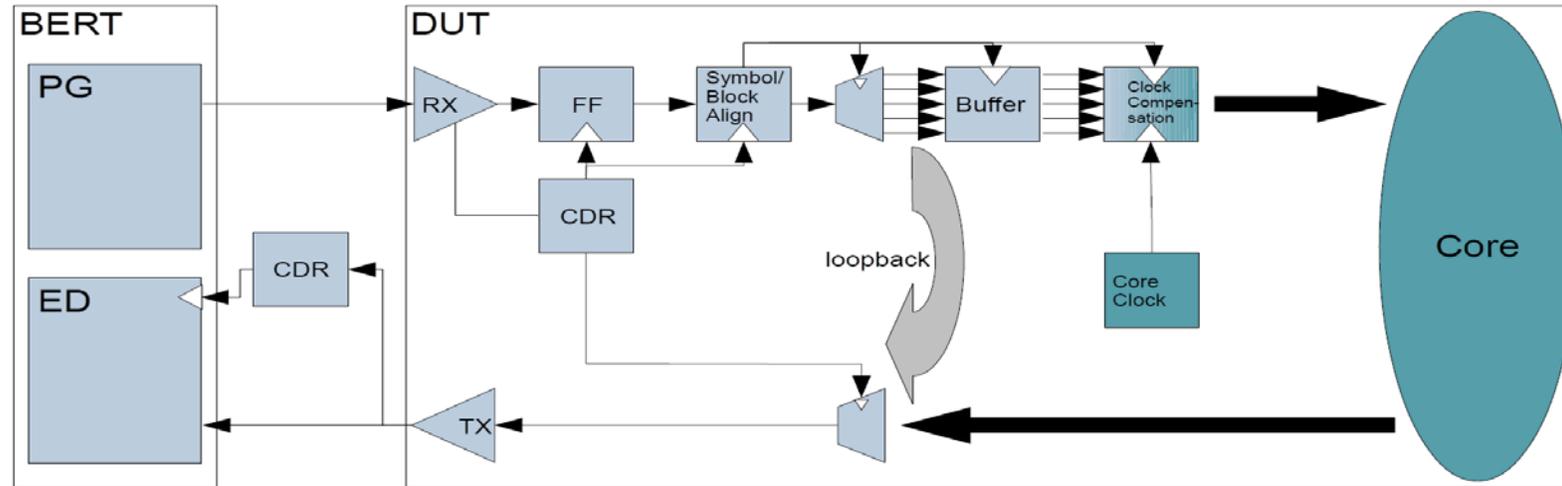


# Loopback - 2

- Modification is within SKPOS only
- BERT ED needs to filter SKPOS on expected as well as received pattern and compare remaining bits
- Not available yet but will be available within August / September 2014
- What if testing is required in the meantime?



# Loopback – Near End Loopback



If chipset control is possible use near end loopback

- Near end loopback bypasses the clock compensation and both the DUT RX as well as the DUT TX run in the BERT's clock domain
- The DUT does not modify the pattern and normal BER comparison can be used
- BUT since the DUT uses the clock recovered by the RX to clock the TX jitter is transferred back to the BERT ED. Choose BERT ED clocking with respect to DUT jitter transfer characteristics

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# THANKS



BY  
**NeuHelium**