NeuHelium
新氦类脑智能

类脑智能 驱动未来

逻辑分析仪
16864A

类脑智能 驱动未来

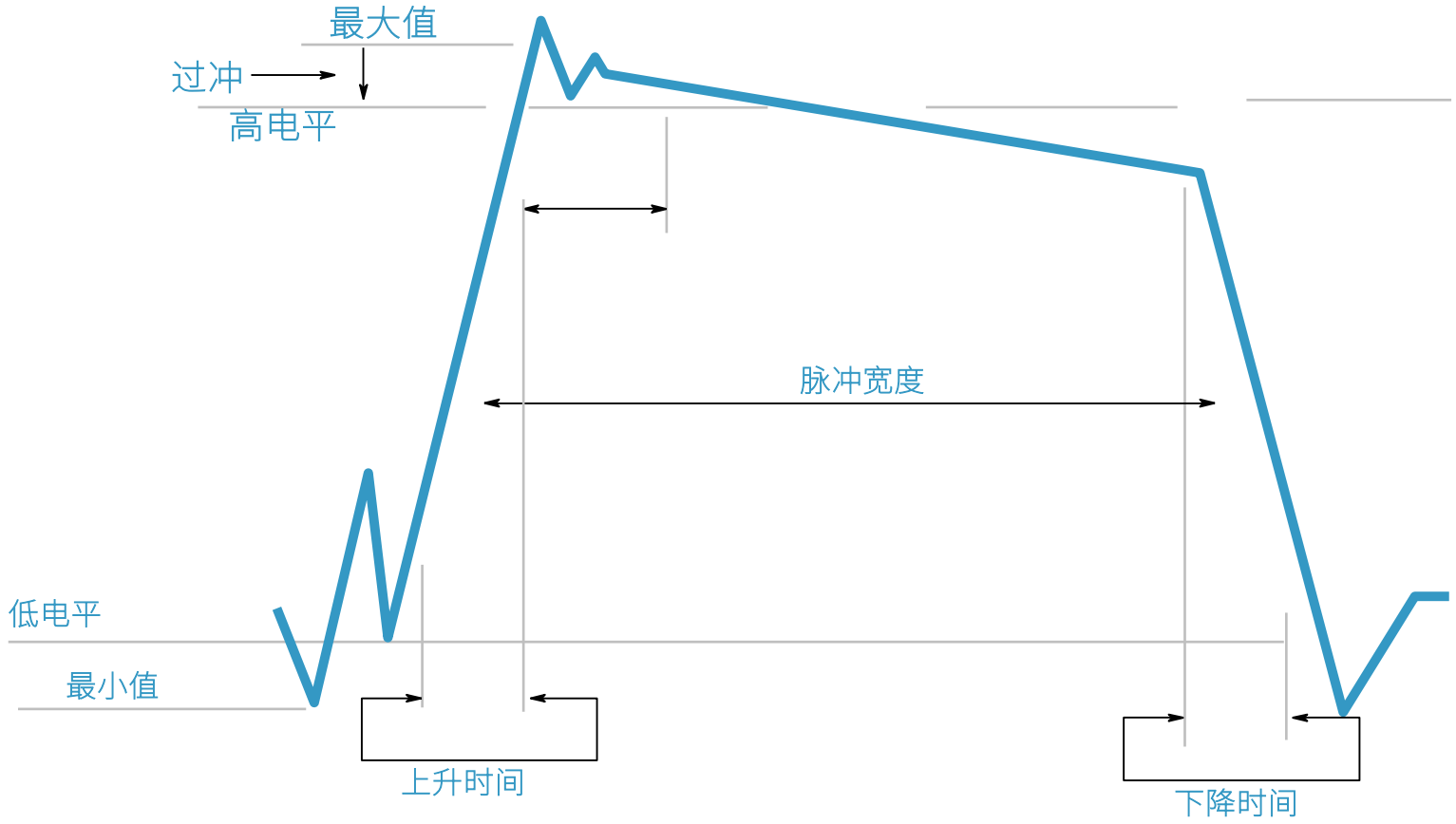
BY
NeuHelium

逻辑分析仪课程内容

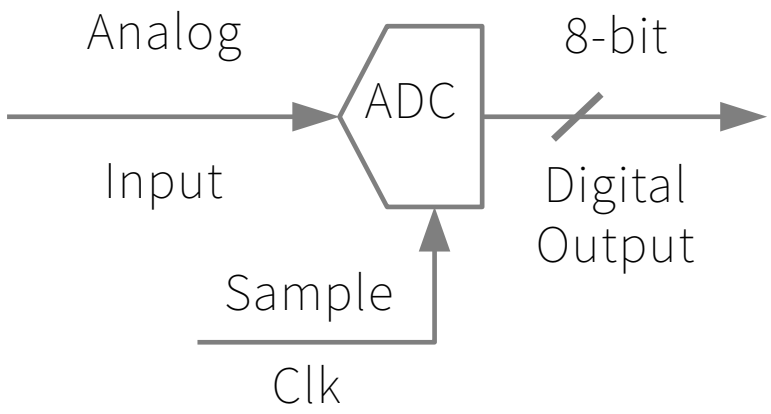
1. 逻辑分析技术
2.逻辑分析仪工作原理
3.逻辑分析仪的触发
4.逻辑分析仪的探头应用
5.逻辑分析仪的测试应用

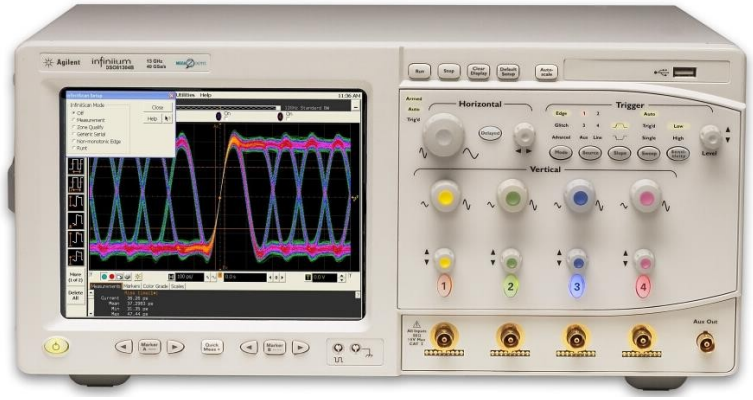
模拟分析

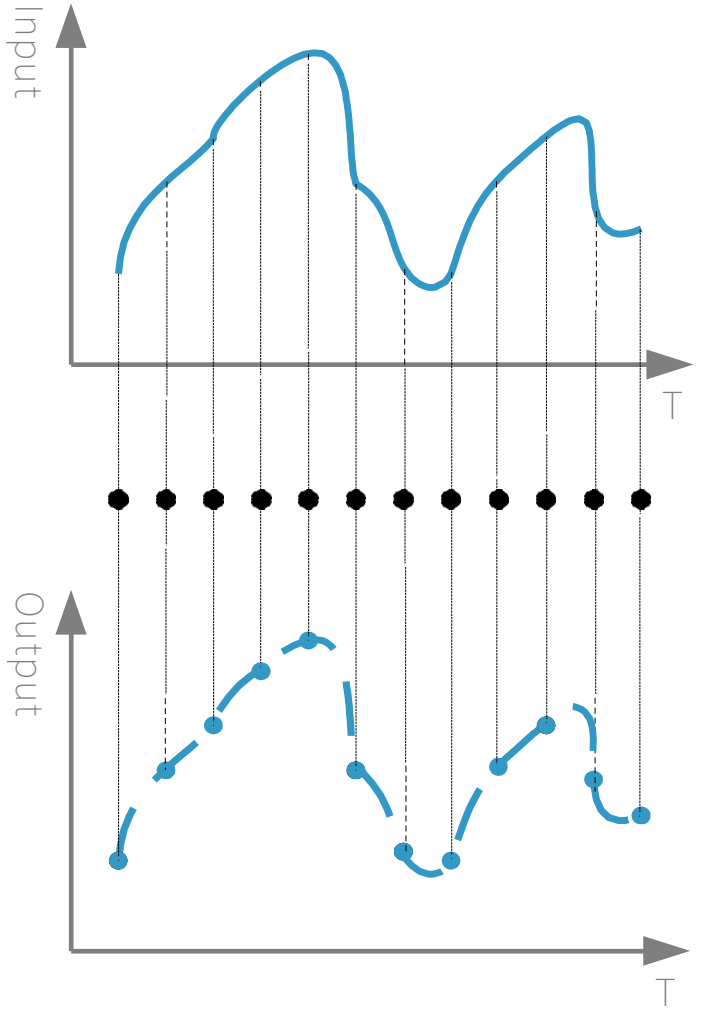
模拟分析指对模拟信号或者数字信号的模拟参数进行分析



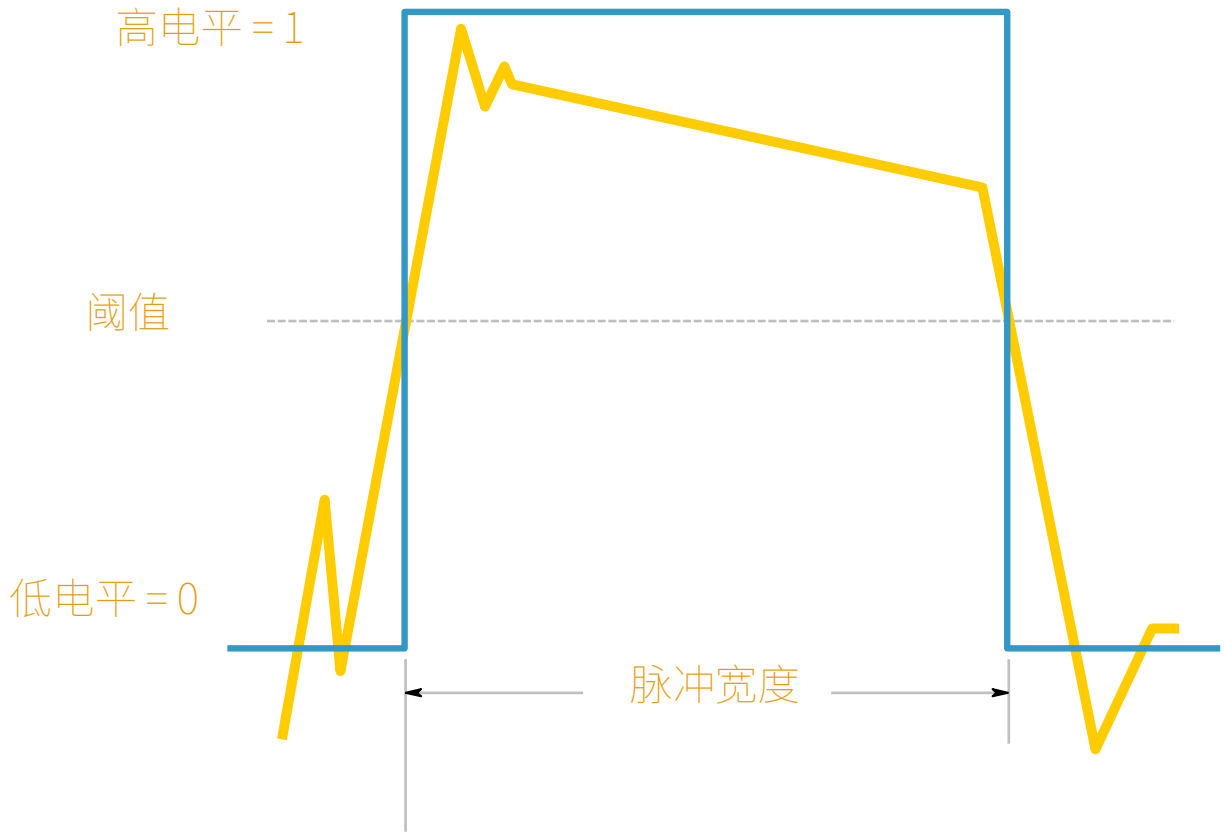
模拟分析使用的工具：示波器



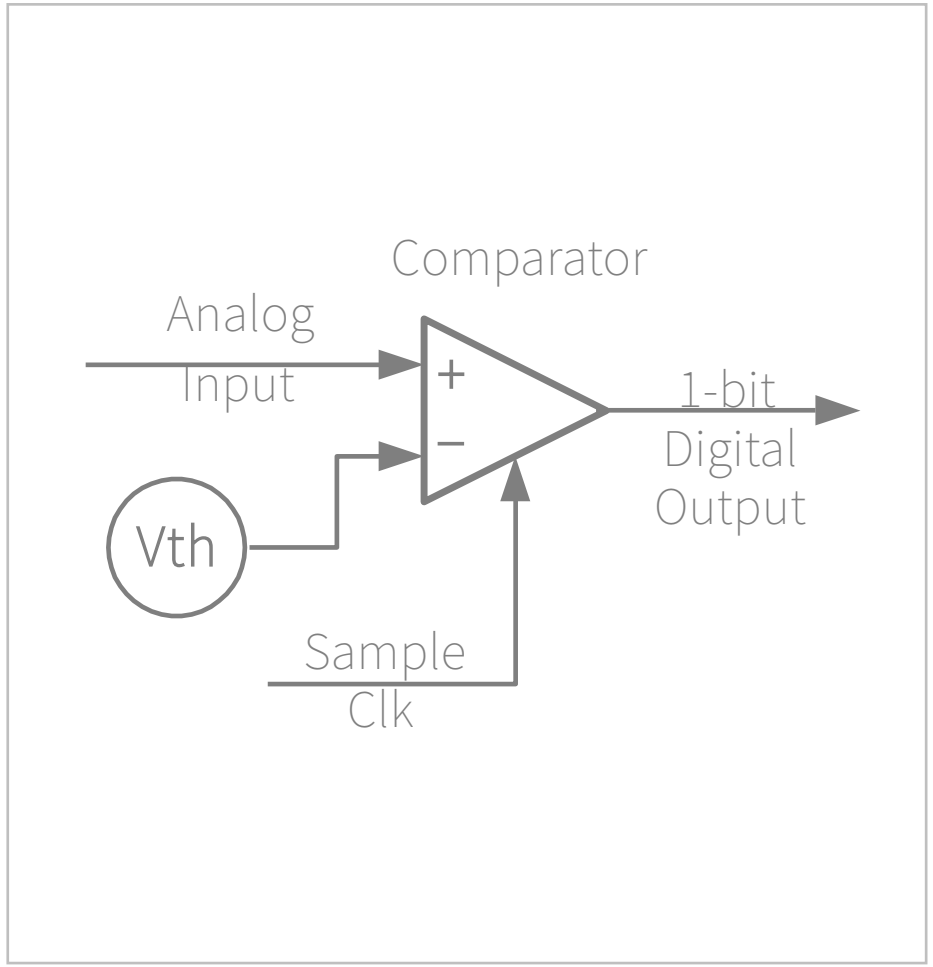


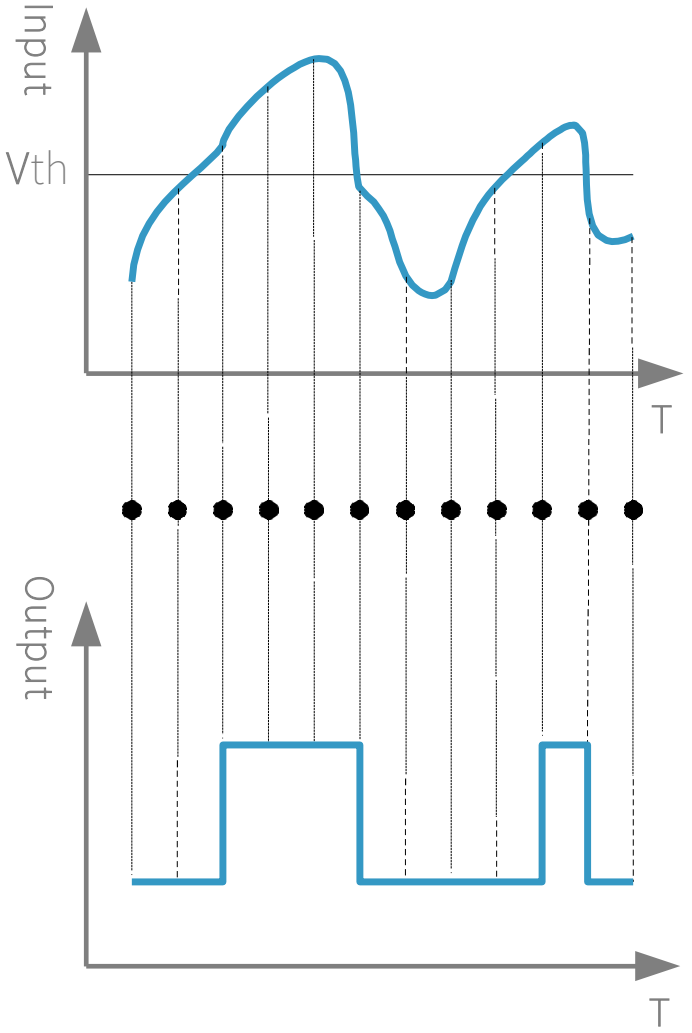


逻辑分析



逻辑分析使用的工具：逻辑分析仪





逻辑分析仪与示波器的区别

逻辑分析仪与示波器相比可以有更多通道，但垂直分辨率只有1bit。

逻辑分析仪与示波器的区别

示　波　器	逻　辑　分　析　仪
• 分析模拟特性	• 分析数字信号
• 比较精确	• 只能区分电平高低
• 测量电压/时间参数	• 检查时序/功能
• 2或4个通道	• 很多通道
• 内部时钟采样	• 内时钟或外时钟采样

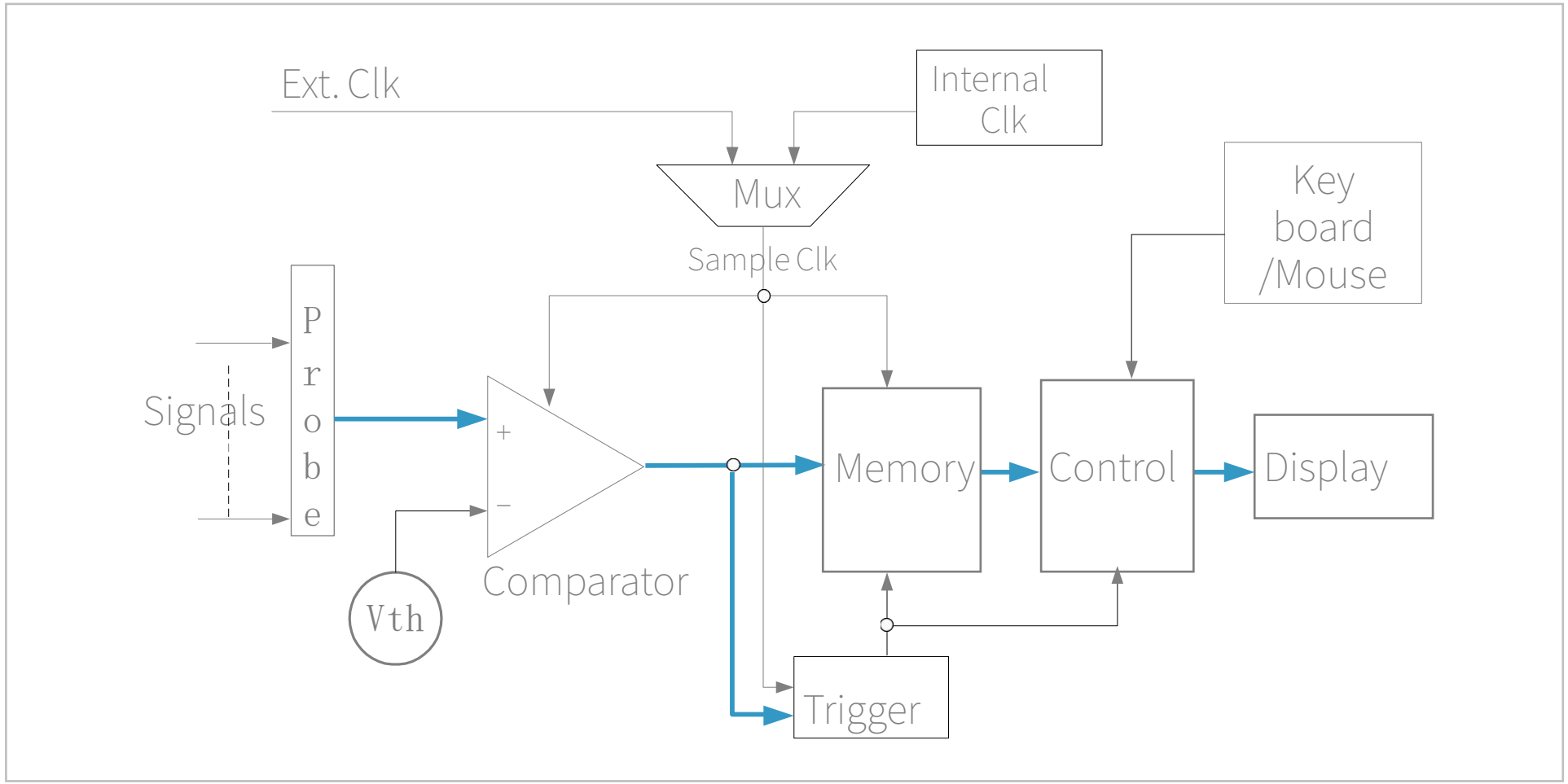
类脑智能 驱动未来

逻辑分析仪课程内容

1. 逻辑分析技术
2.逻辑分析仪工作原理
3.逻辑分析仪的触发
4.逻辑分析仪的探头应用
5.逻辑分析仪的测试应用

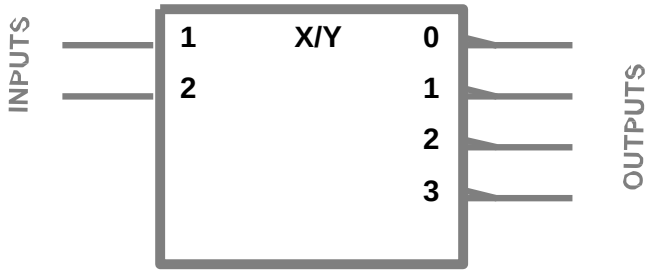
逻辑分析仪的内部结构

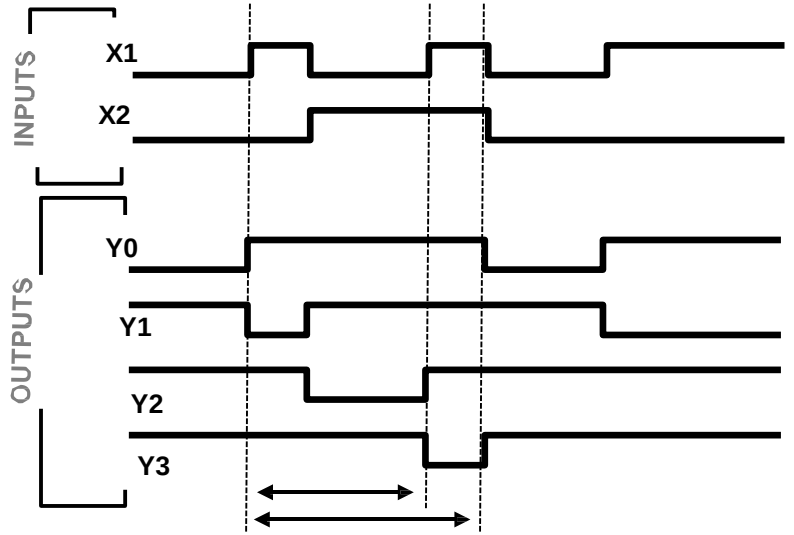
逻辑分析仪结构框图



定时分析的原理?

定时分析指用逻辑分析仪内部时钟对输入信号采样

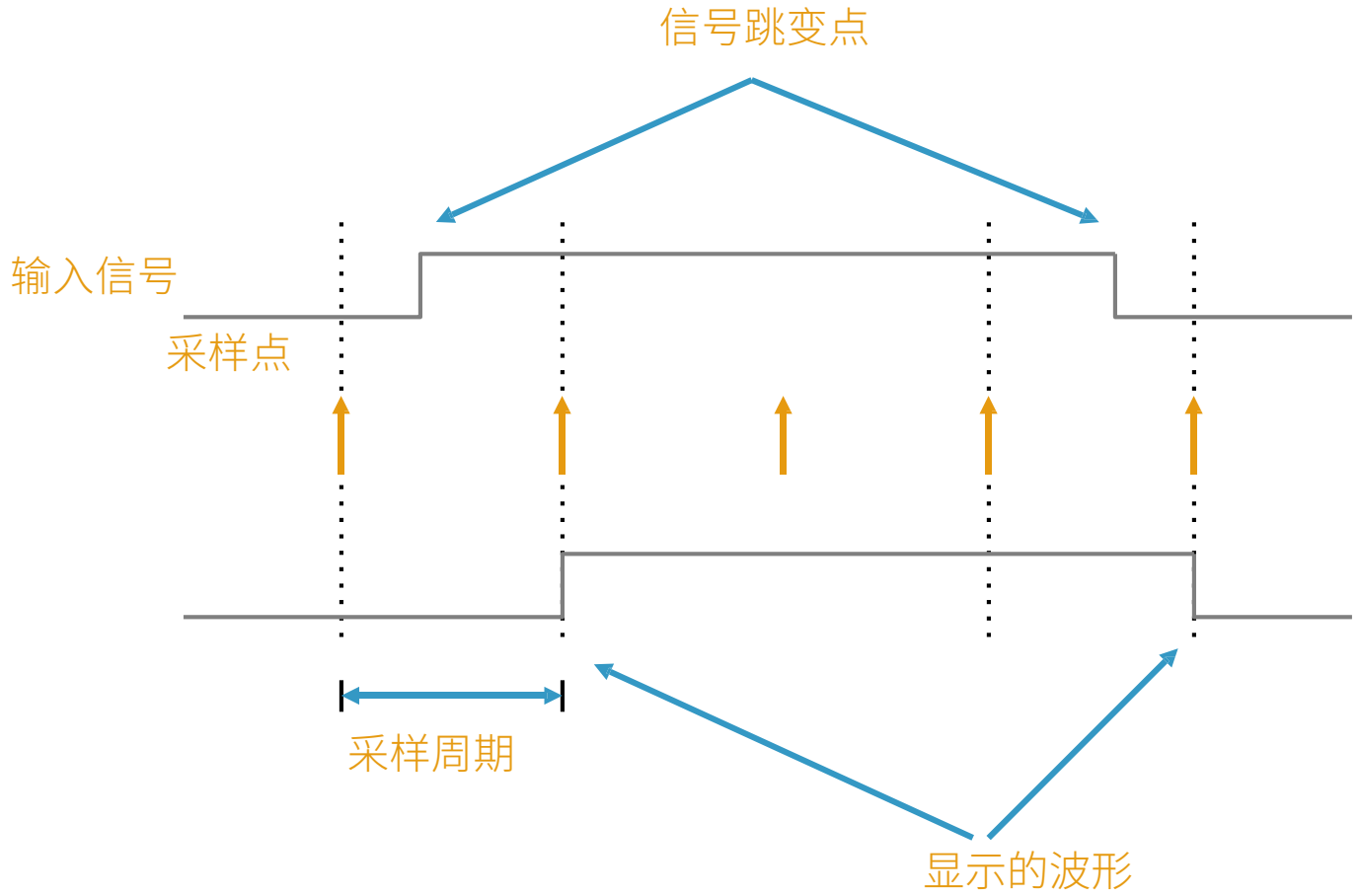




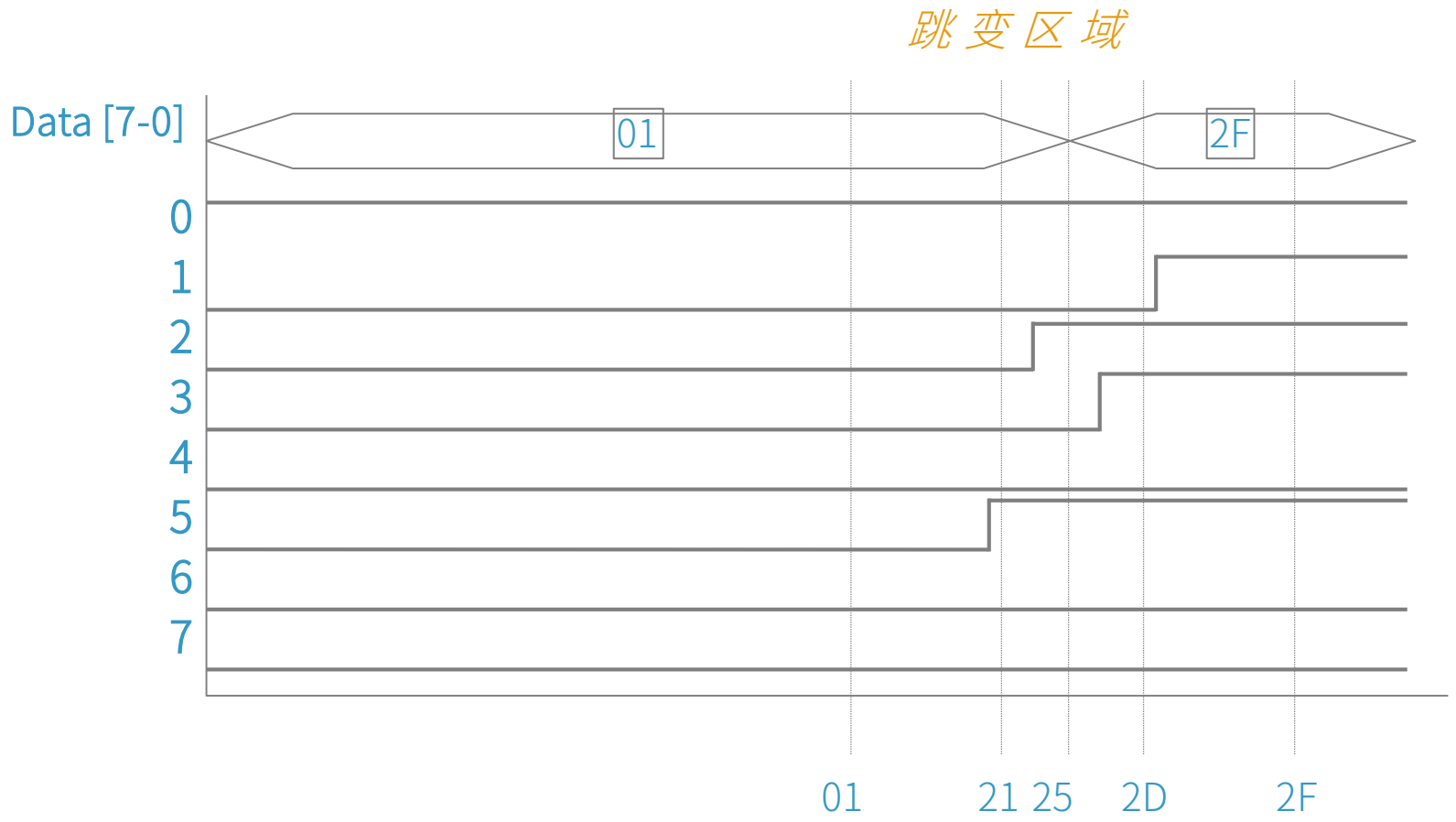
逻辑分析仪 → 采样时钟

定时分析的精度

时间精度取决于采样率



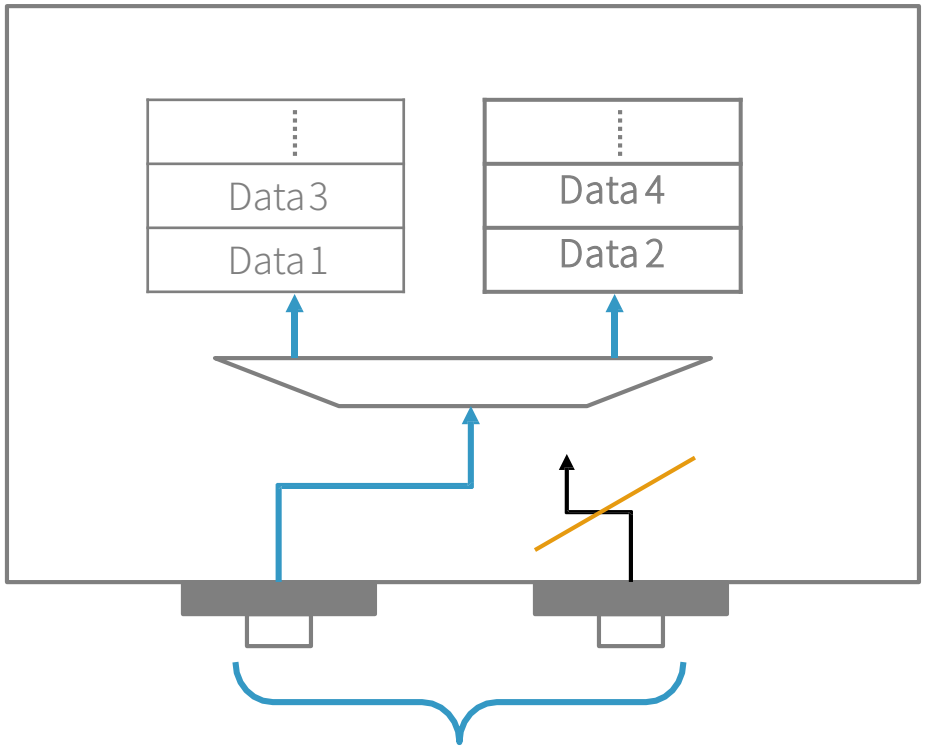
用定时分析模式分析总线跳变



提高定时分析速率的方法

半通道模式：

- 采样率翻倍
- 存储深度翻倍
- 有效通道减半

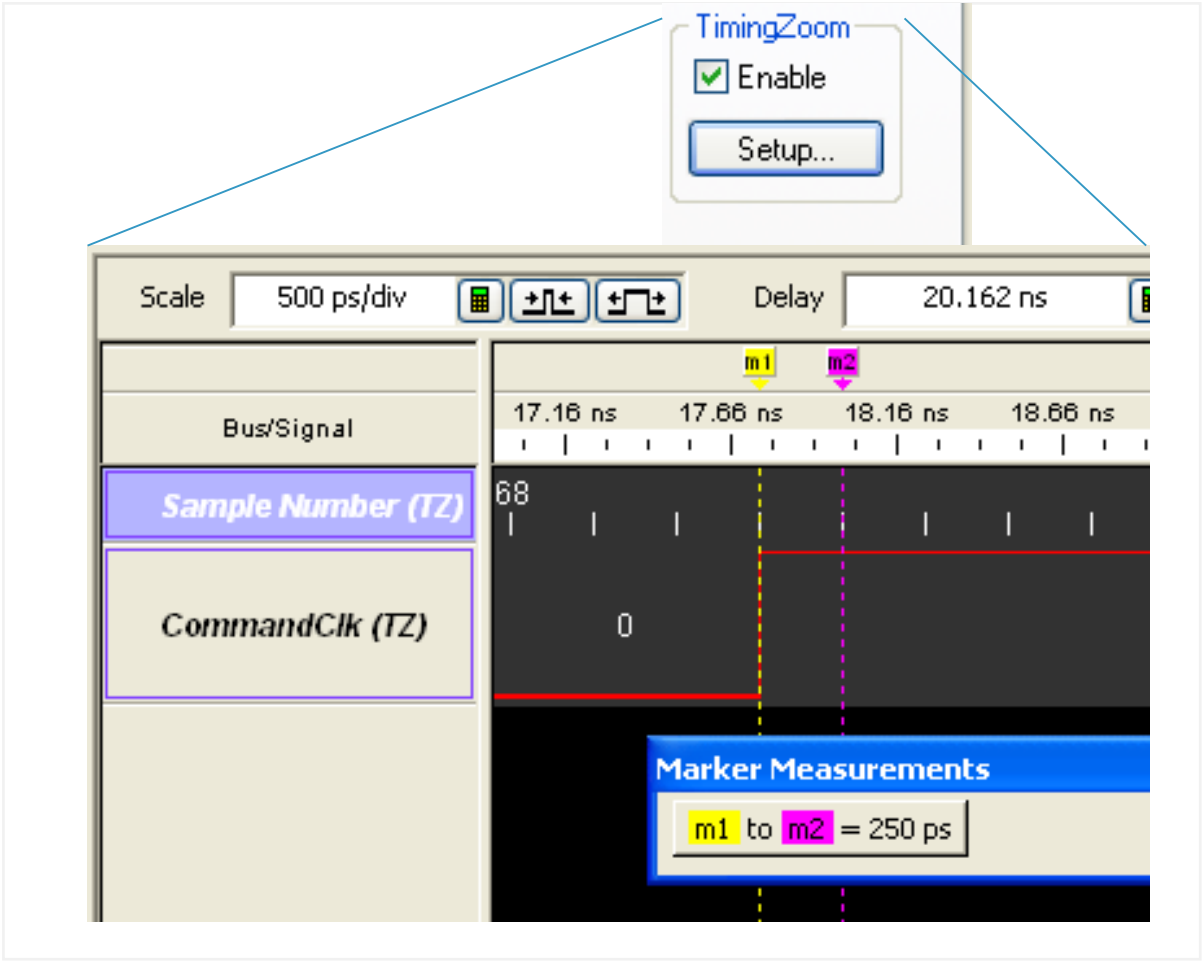


逻辑分析仪的一对POD

提高定时分析速率的方法

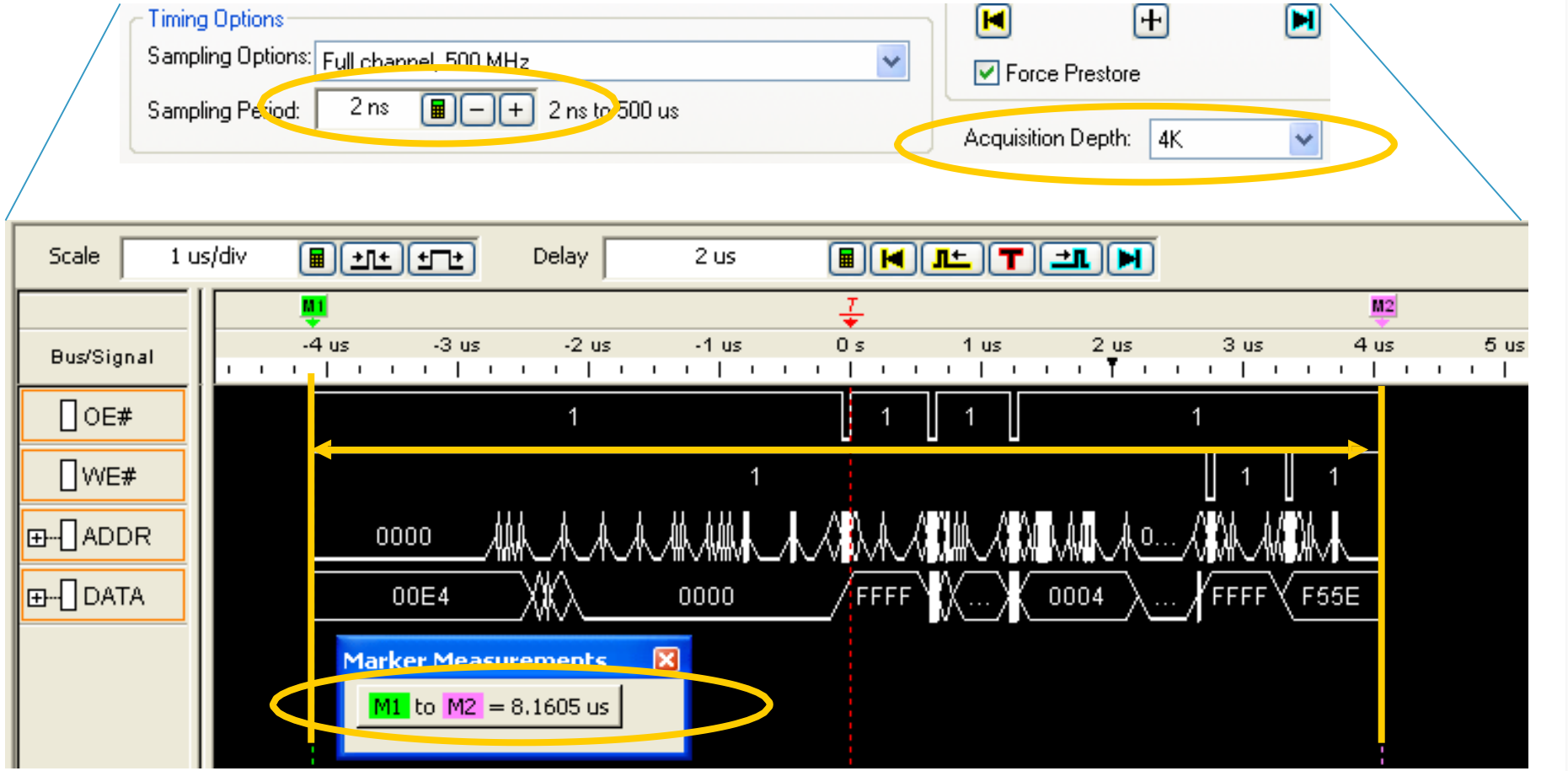
Timing Zoom：

- 高速采样（4G Sa/s）
- 只有64k存储深度
- 可以和正常定时模式同时工作



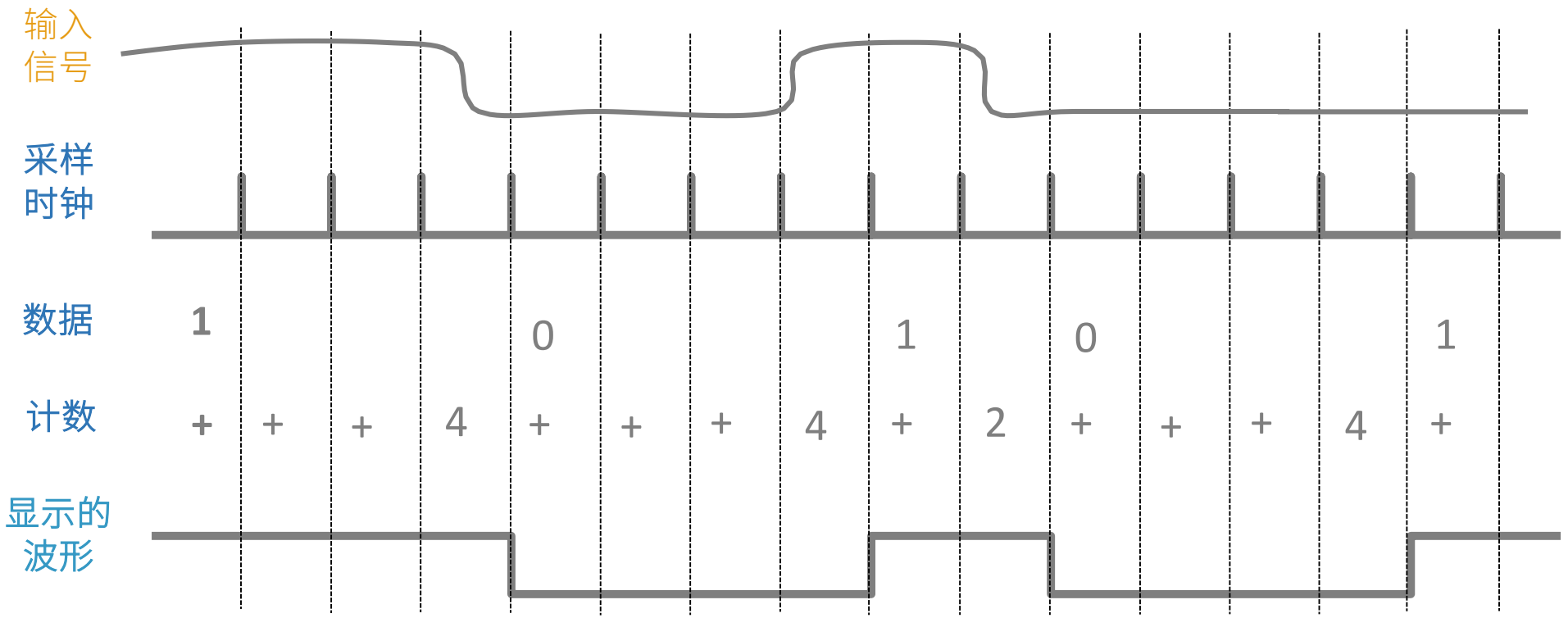
定时分析记录的波形长度

记录波形时间 =采样周期 ×内存深度



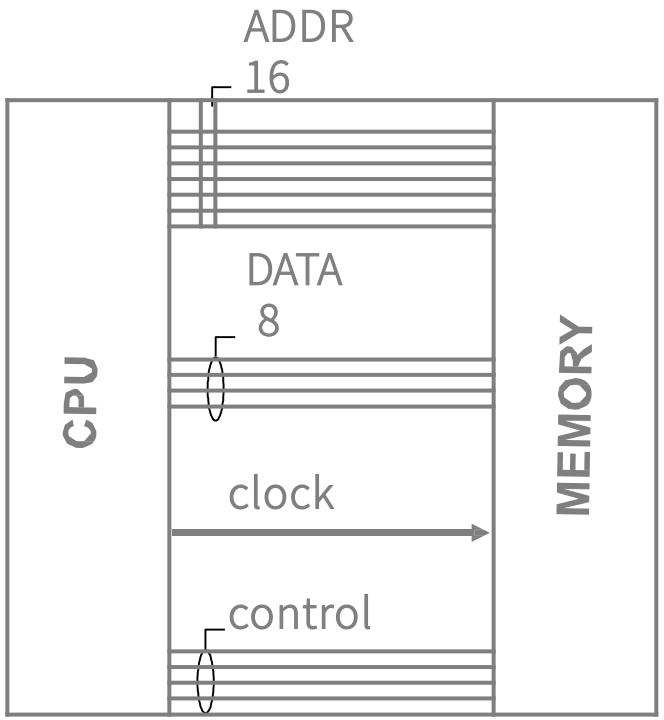
增加记录时间的方法

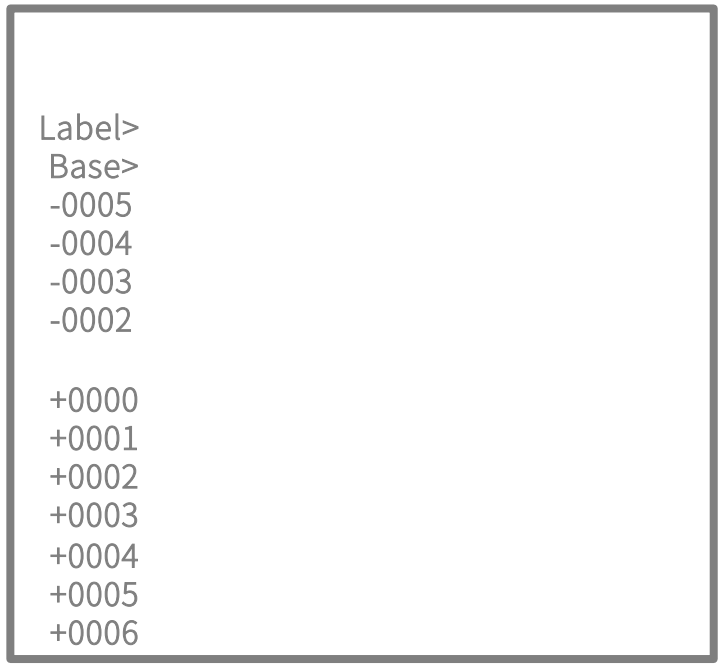
跳变定时模式：只在输入信号发生跳变时进行记录



什么是状态分析?

Track Functional Problems

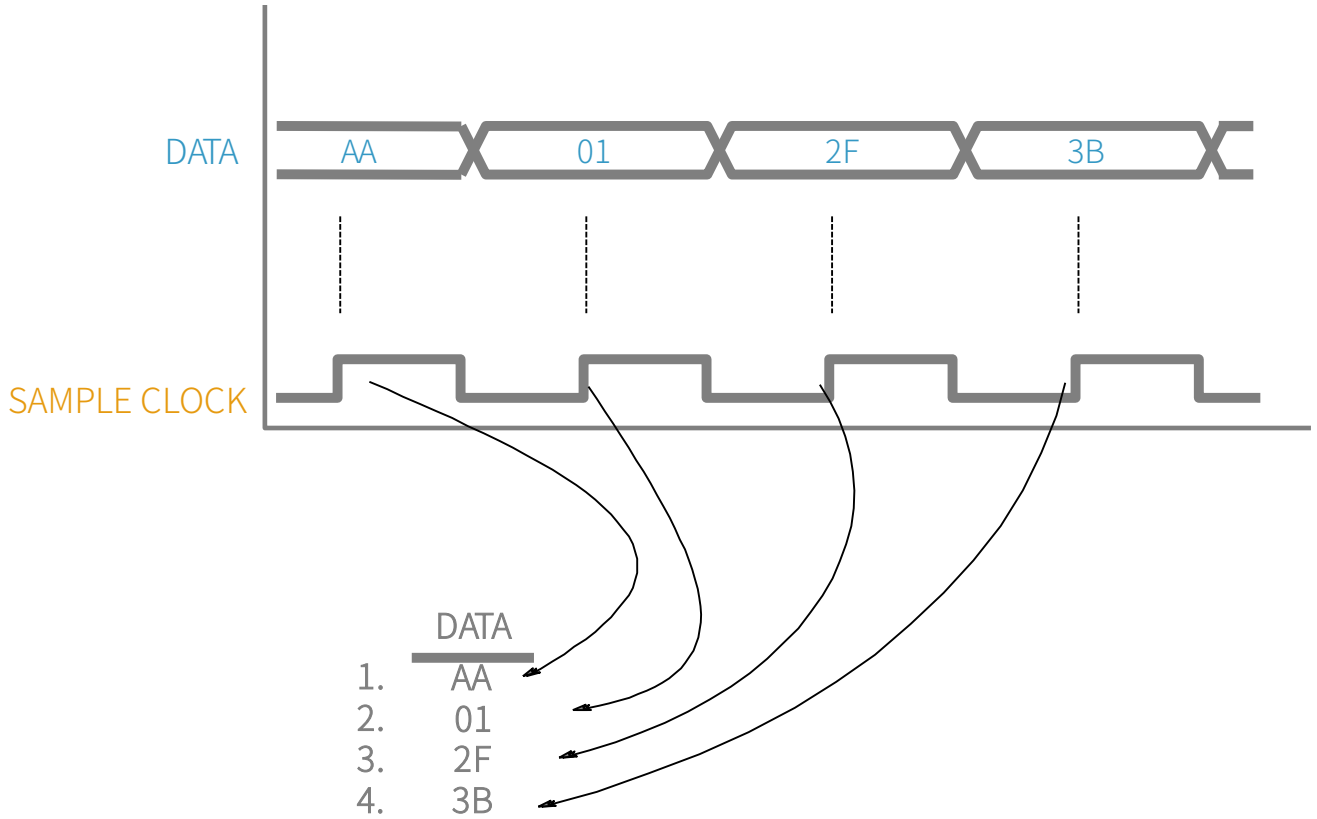




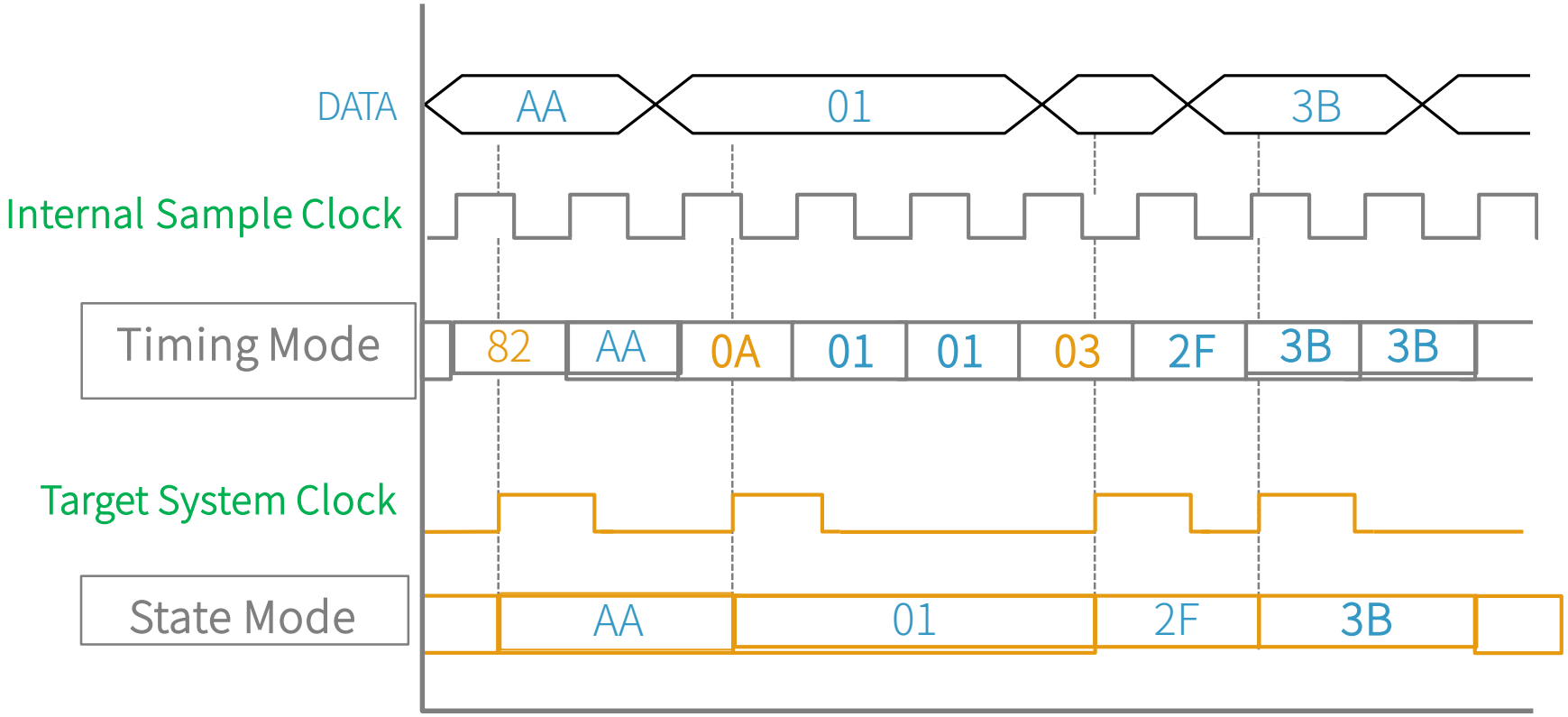
Measurement

状态分析

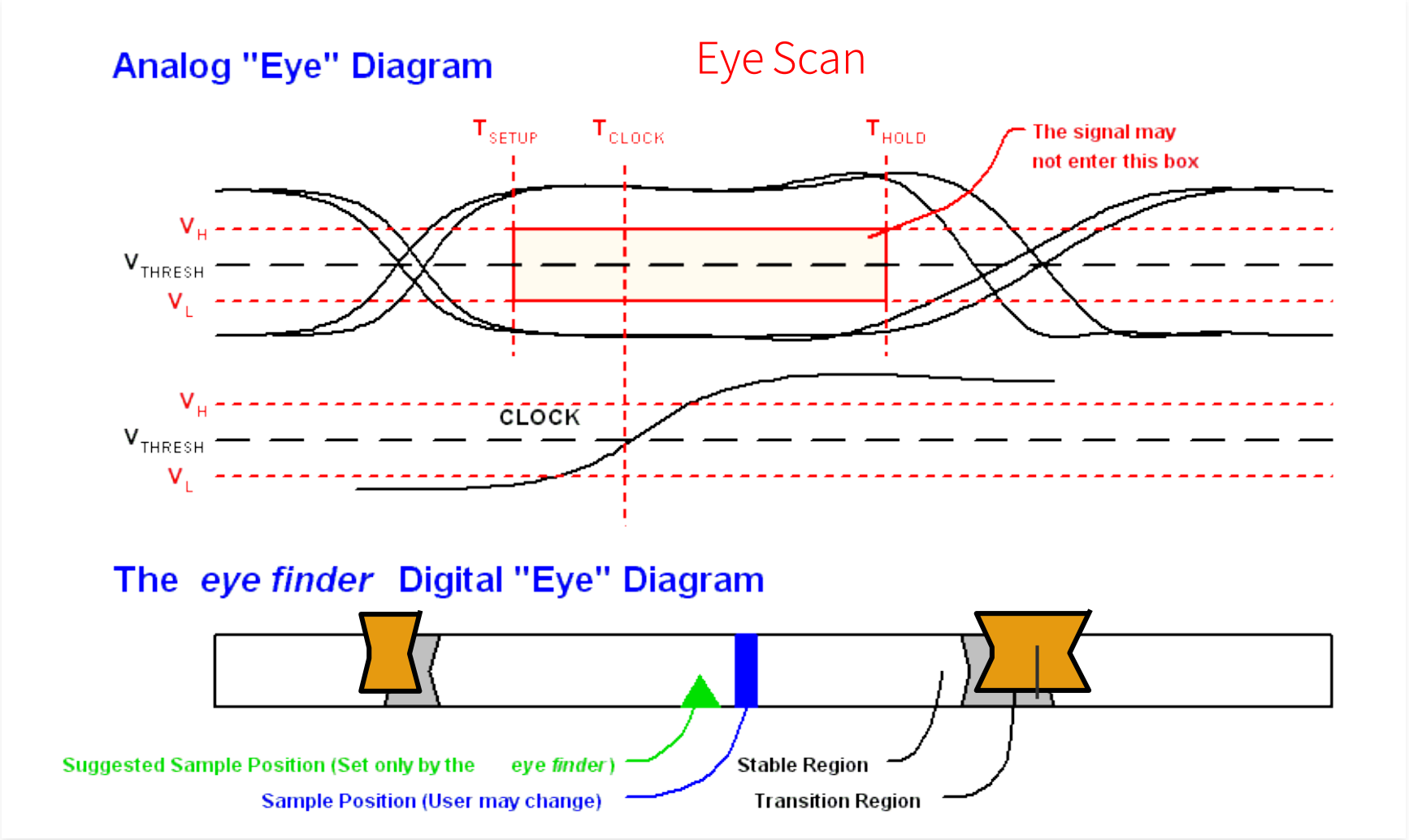
状态分析的采样时钟来源于被测设备，所以是可 以和数据同步的。



定时分析vs. 状态分析?

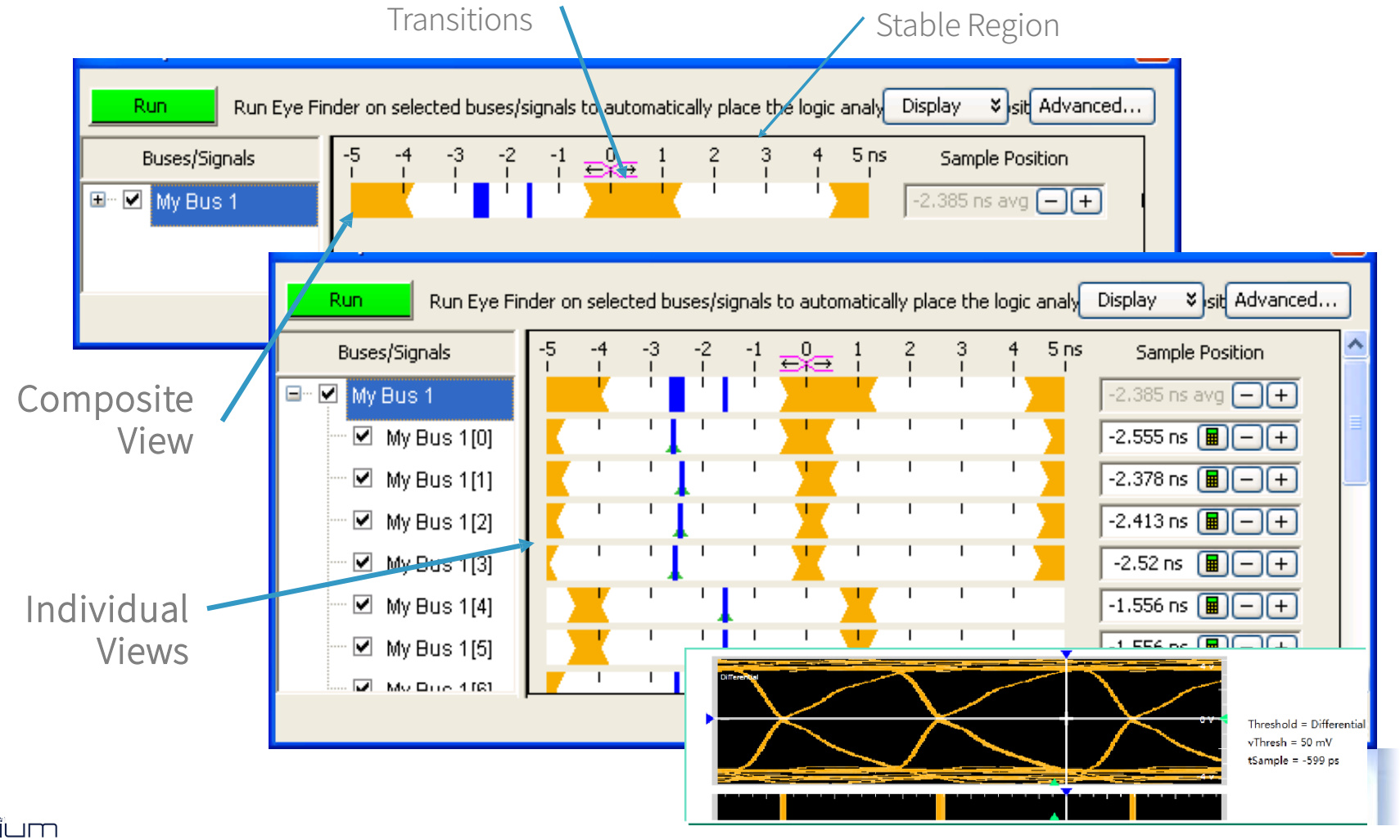


状态分析下建立/保持时间的调整



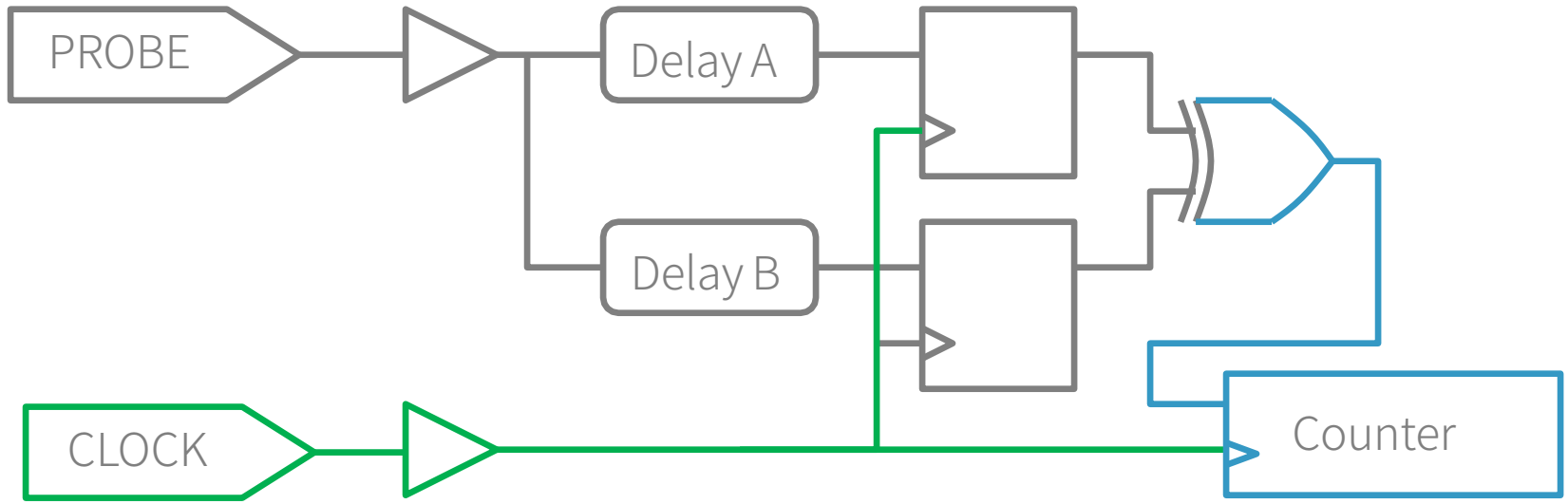
状态分析下建立/保持时间的调整

EyeScan 的运行结果



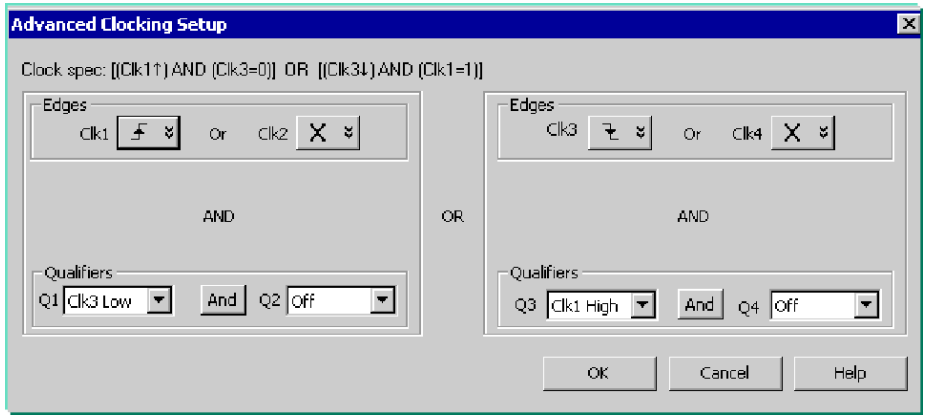
状态分析下建立/保持时间的调整

Eye Scan的工作原理?



状态分析的时钟

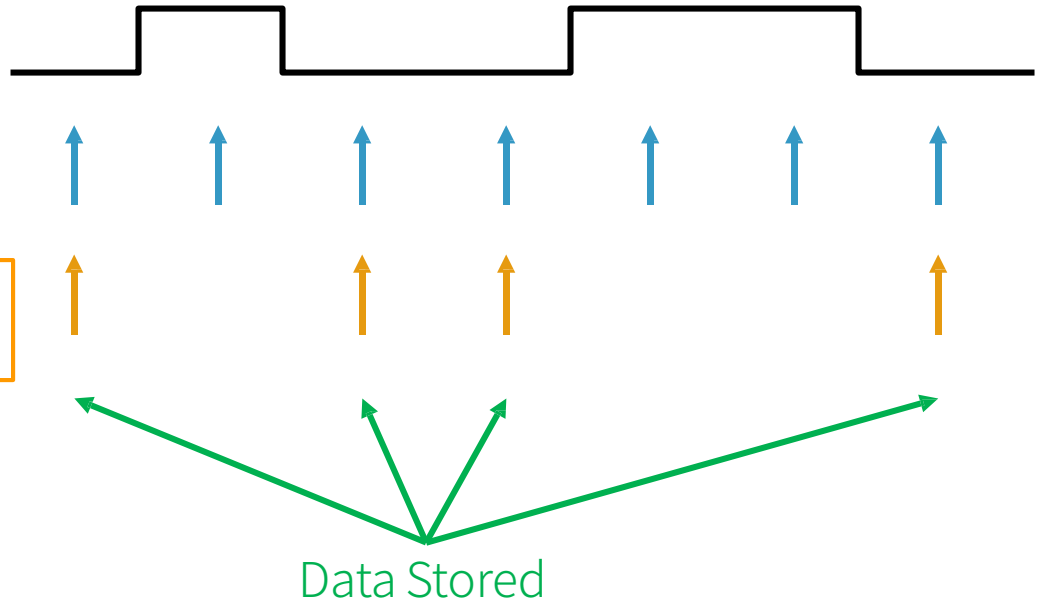
时钟限定



CLK Qualifier (K)

Sampling CLK (J)

Qualified Clocks
(J) AND (K=0)



逻辑分析仪课程内容

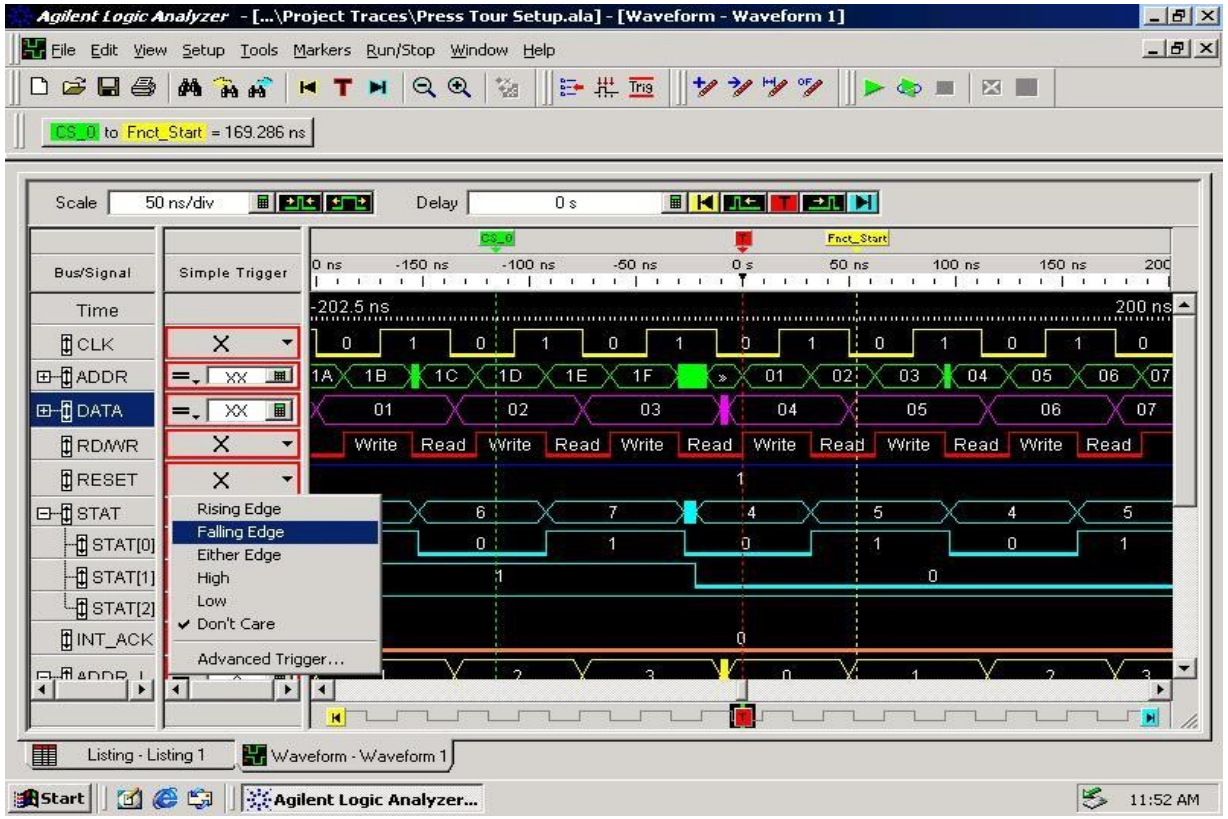
1. 逻辑分析技术
2.逻辑分析仪工作原理
3.逻辑分析仪的触发
4.逻辑分析仪的探头应用
5.逻辑分析仪的测试应用

触发的分类

单步的：简单触发

Common trigger events

- rising edge
- falling edge
- pattern
- Level
- Symbol

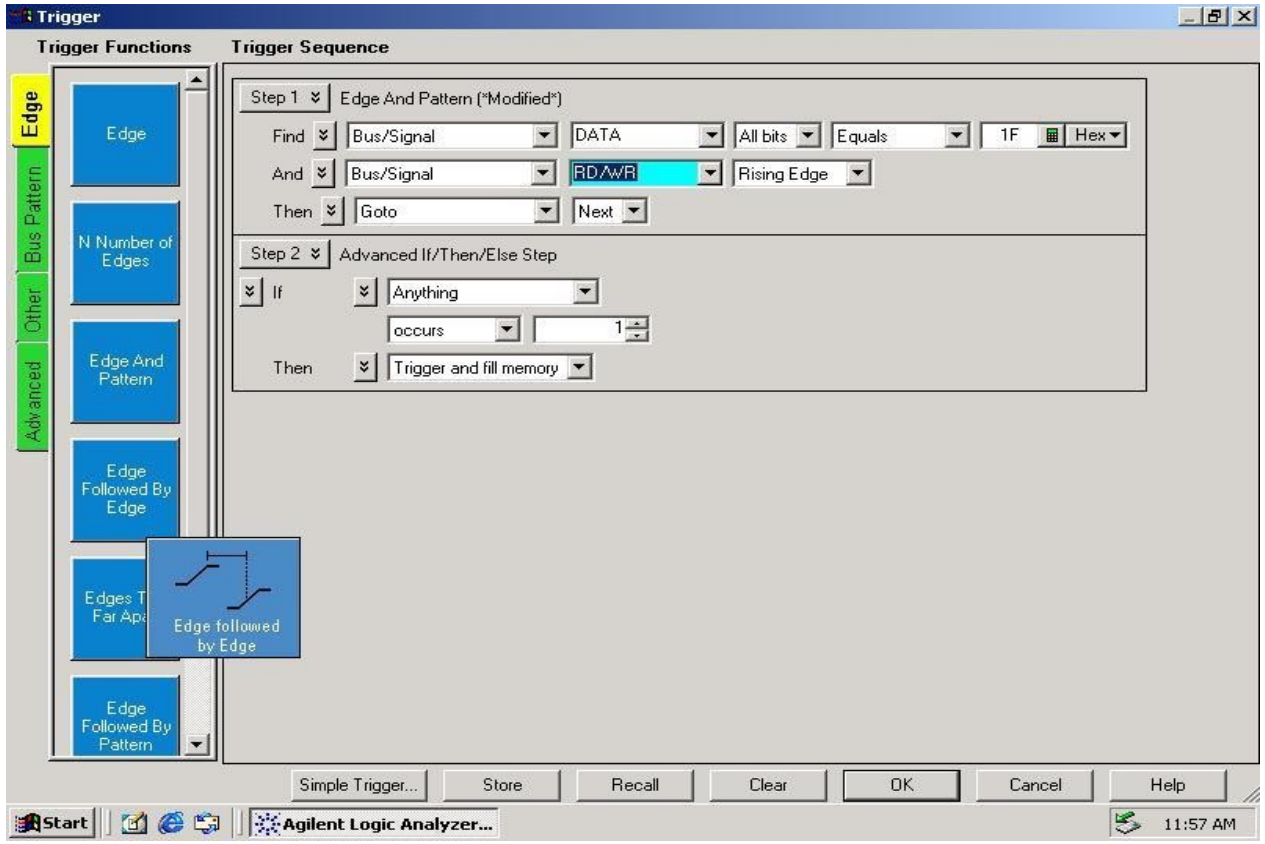


触发的分类

多步的：高级触发

Fast custom triggering with:

- Drag-and-drop
- Graphical views
- Sentence-like structures

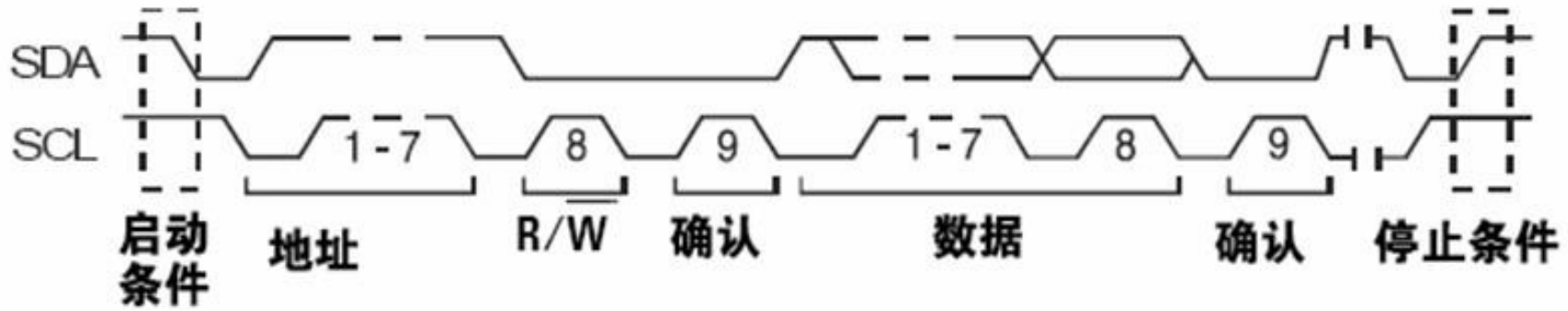


触发举例—I2C总线测量

Lab:试着用触发抓到一个I2C总线的读周期?

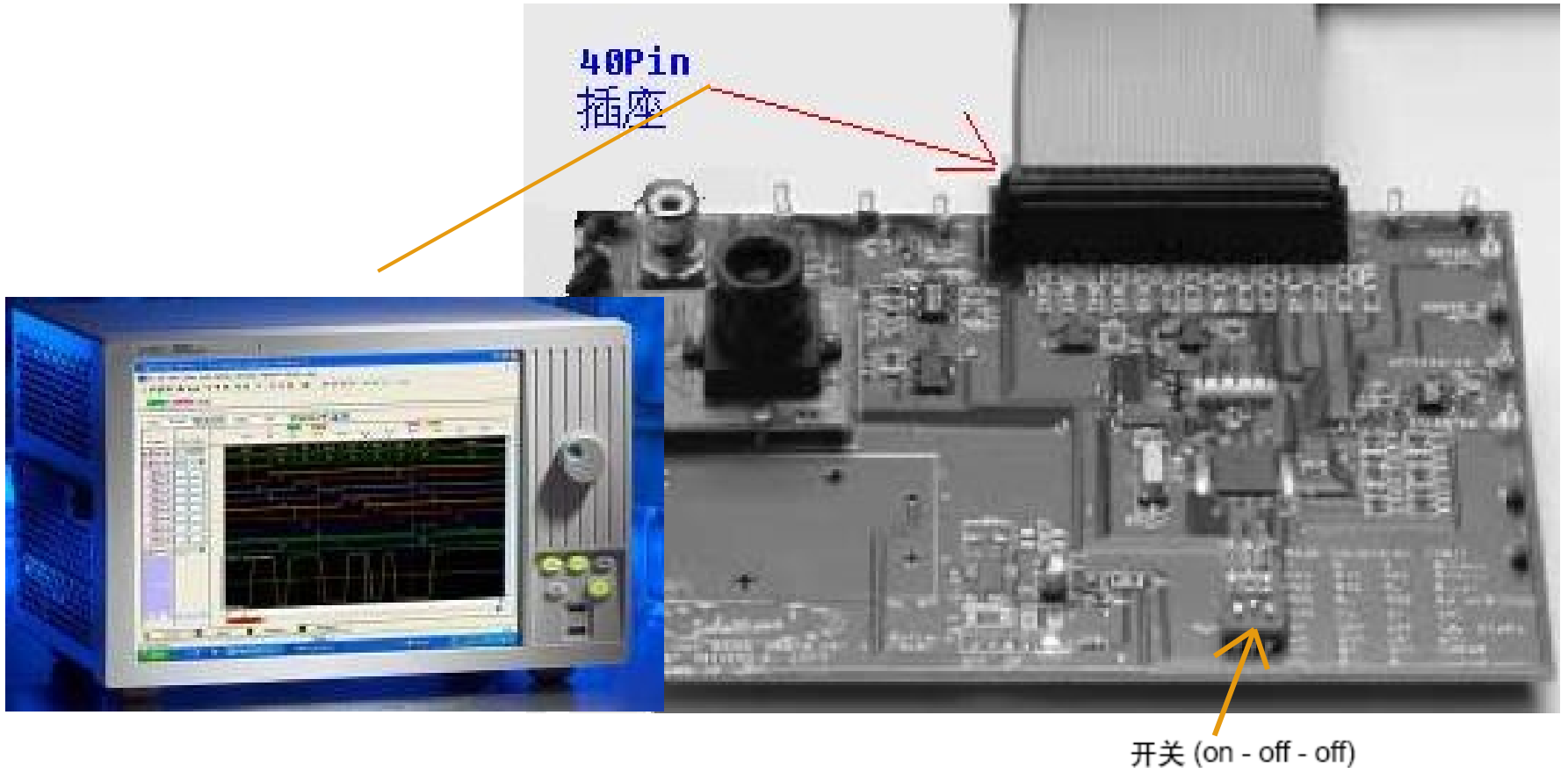
Start Condition（启动条件）：当 SCL 时钟为高而 SDA 数据从高到低转换时

Stop Condition（停止条件）：当时钟 (SCL) 为高而数据 (SDA) 从低到高转换时



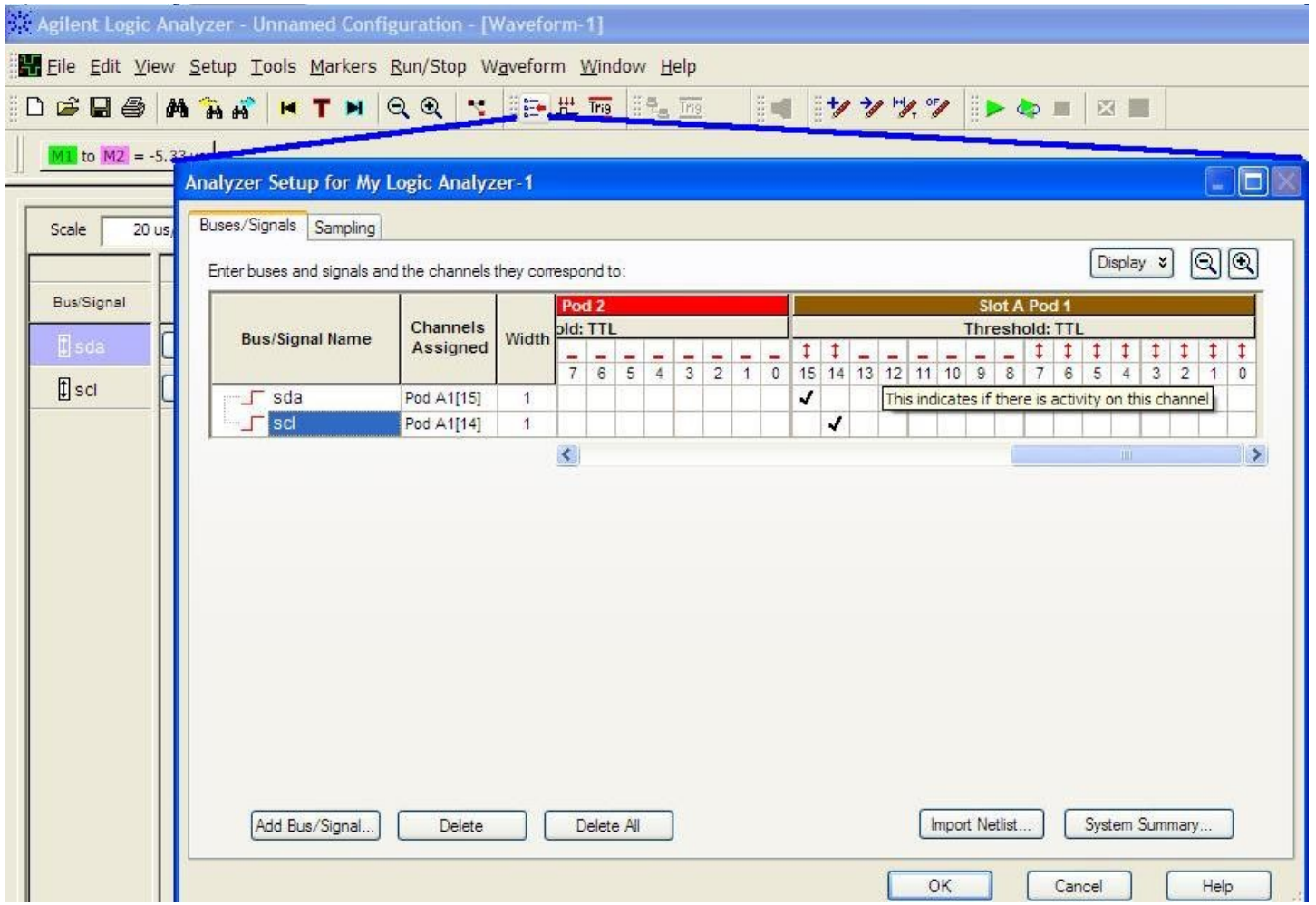
触发举例—I2C总线测量

1、把16800的POD1直接连接至DEMO板的40Pin插座上，开 关设置成（on-off-off）状态



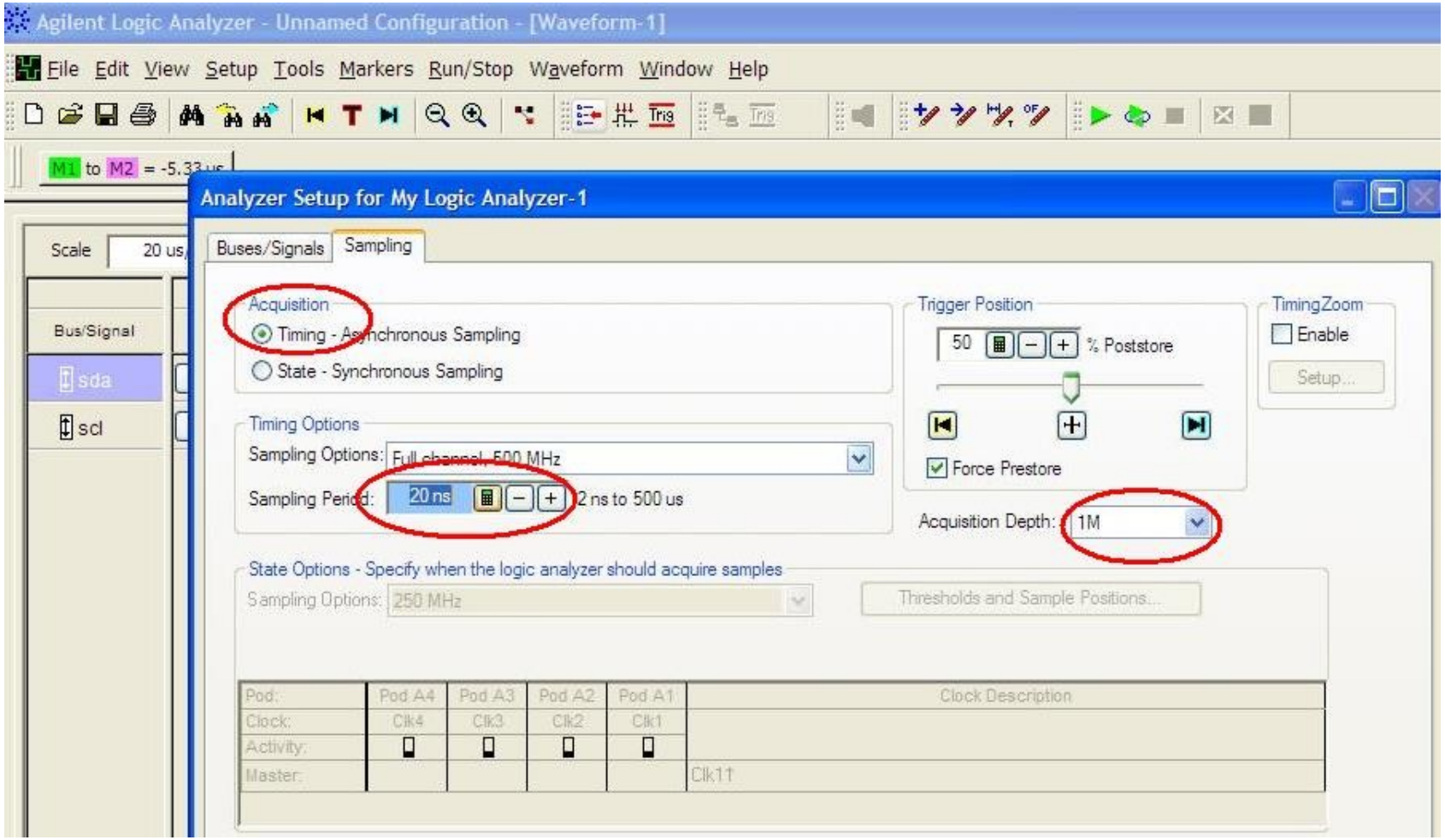
触发举例—I2C总线测量

2、在Bus/Signal Setup菜单下进行信号定义



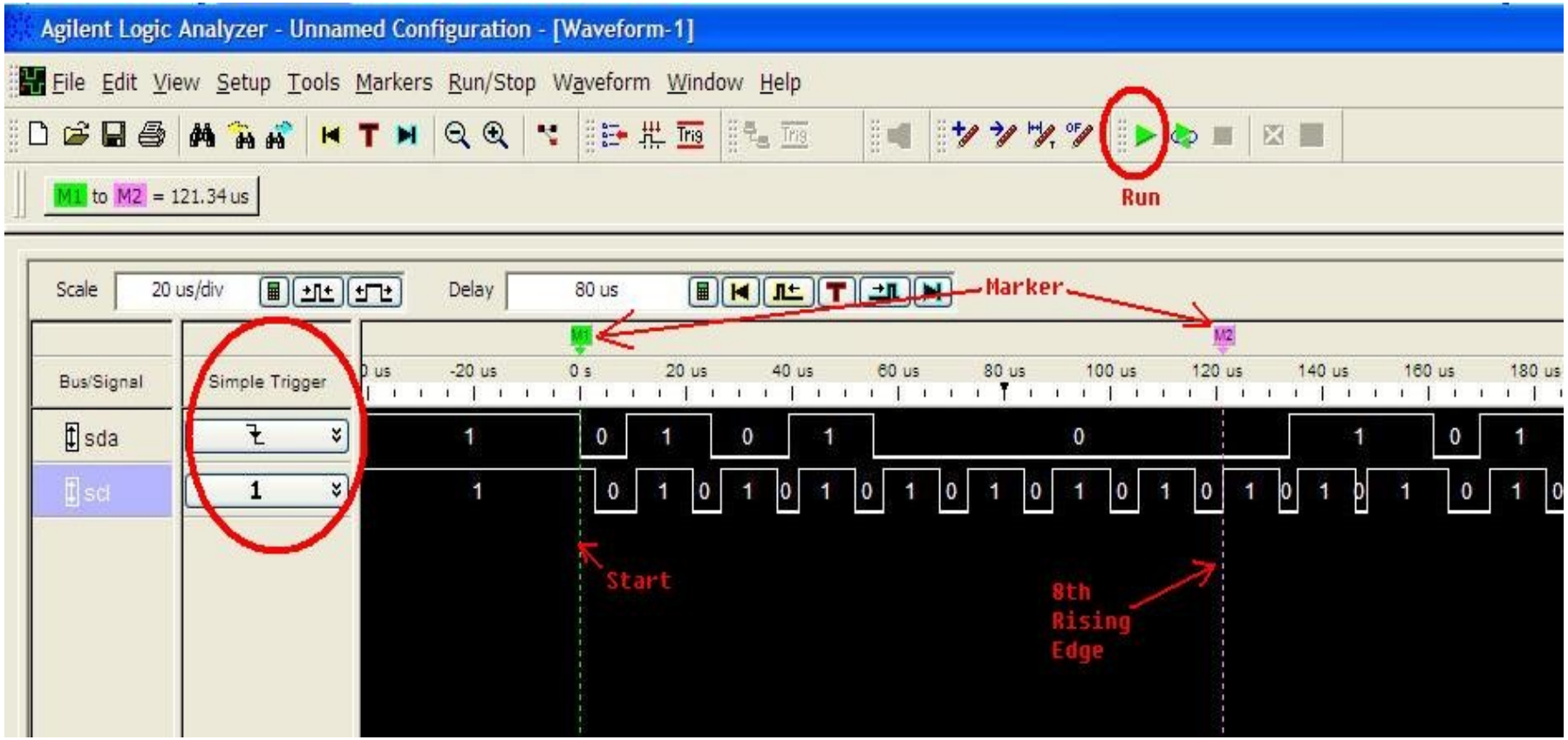
触发举例—I2C总线测量

3、在Sampling Setup菜单下设置采样模式、采样周期、内存深度



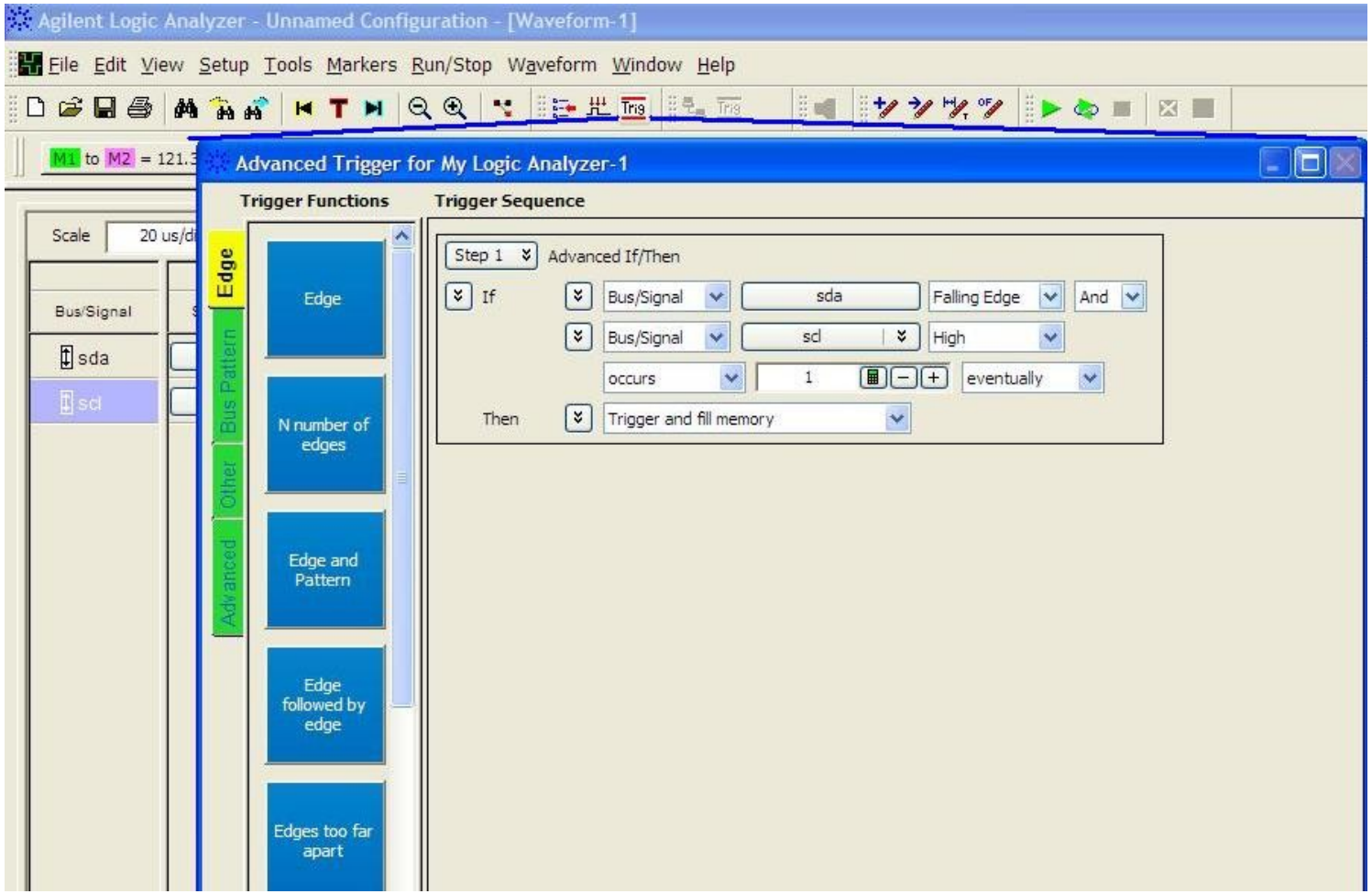
触发举例—I2C总线测量

4、按I2C总线的起始条件设置触发，运行抓到一段波形；从 起始位置数第8个上升沿，可以看到这是一个写时序。



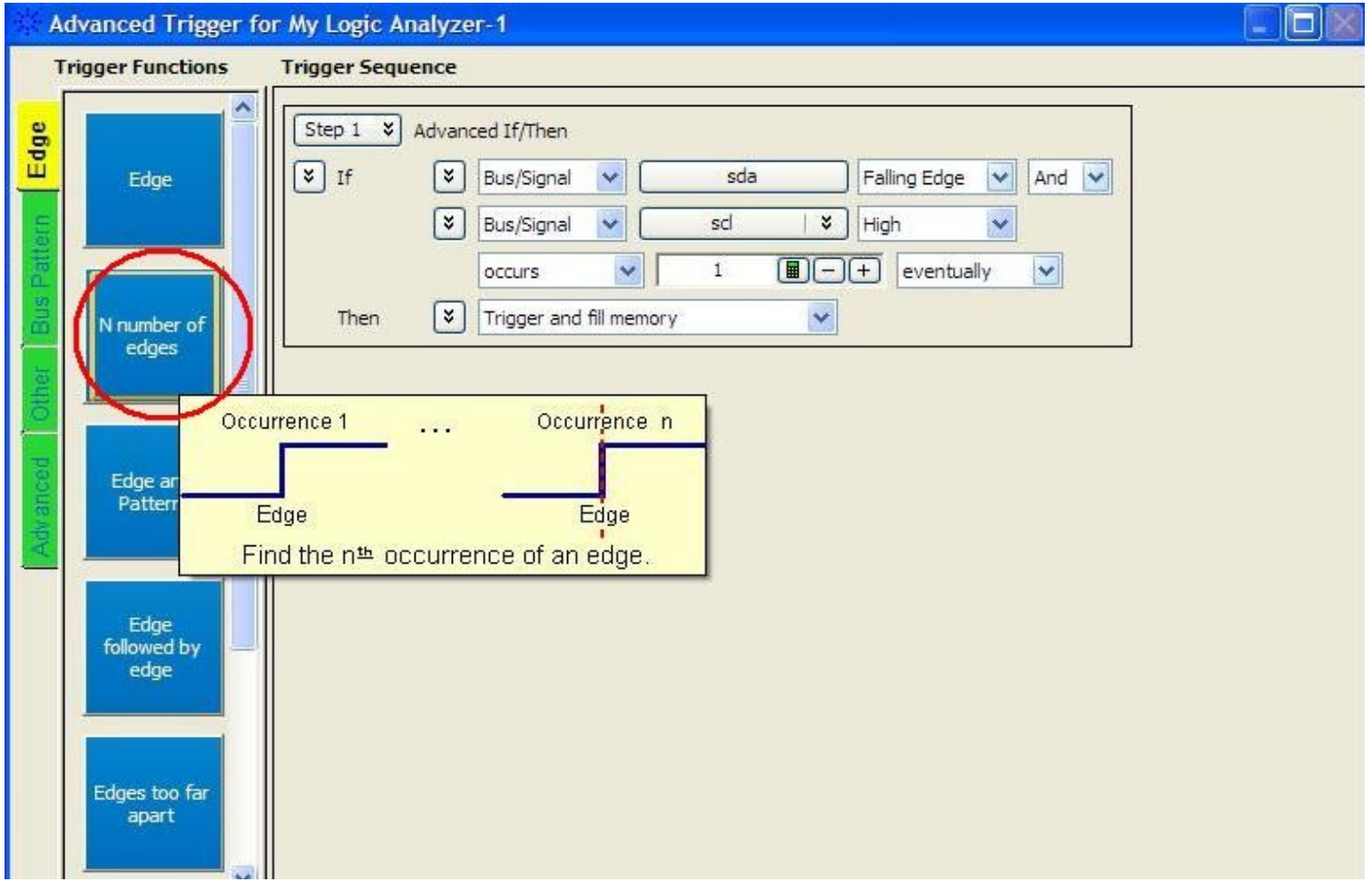
触发举例—I2C总线测量

5、点击Trigger Setup按钮进入高级触发的设置，可以看到刚才设置的触发条件。



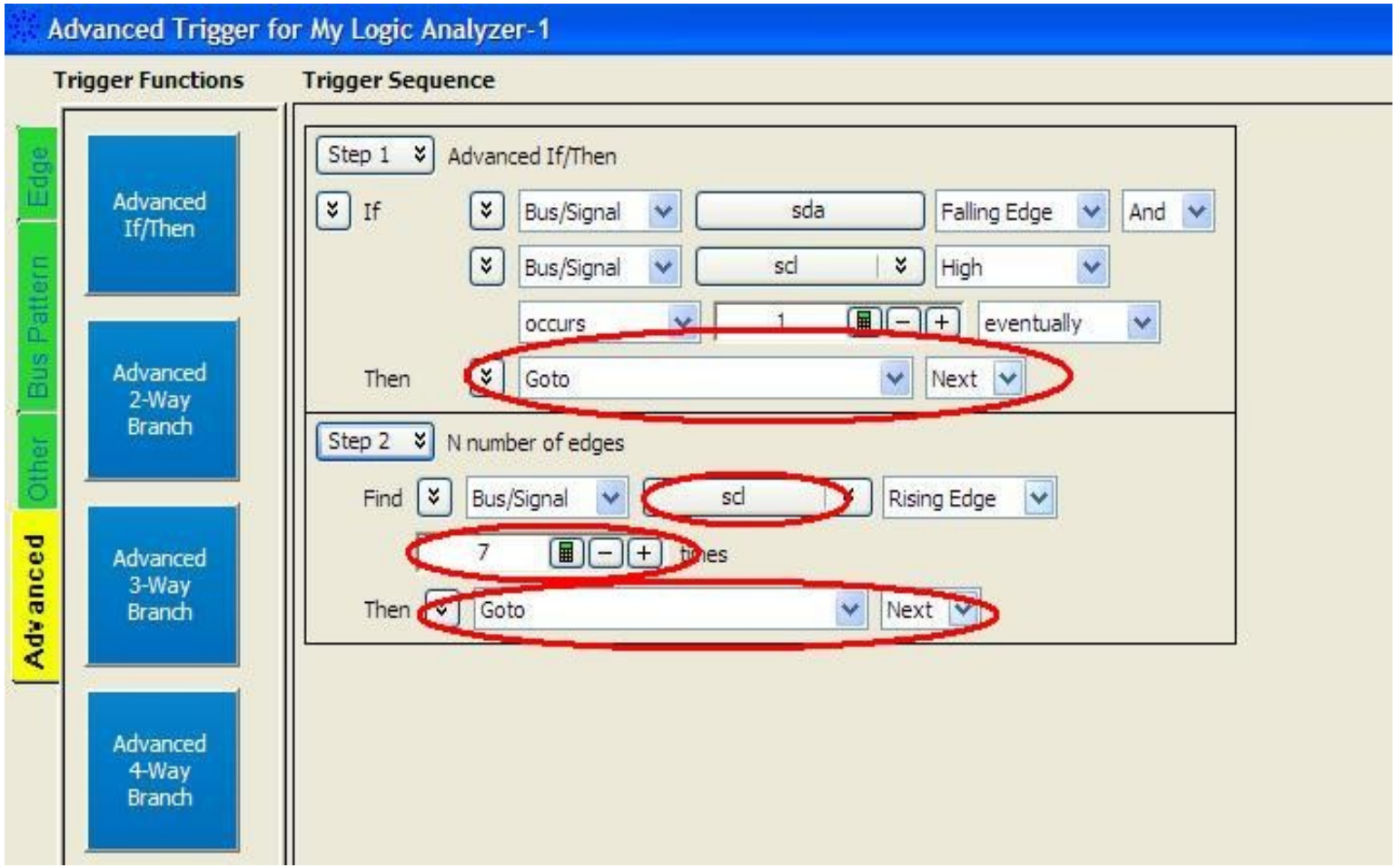
触发举例—I2C总线测量

6、从左边的触发功能中找到”N number of edges”的触发， 拖到刚才触发函数的下面。



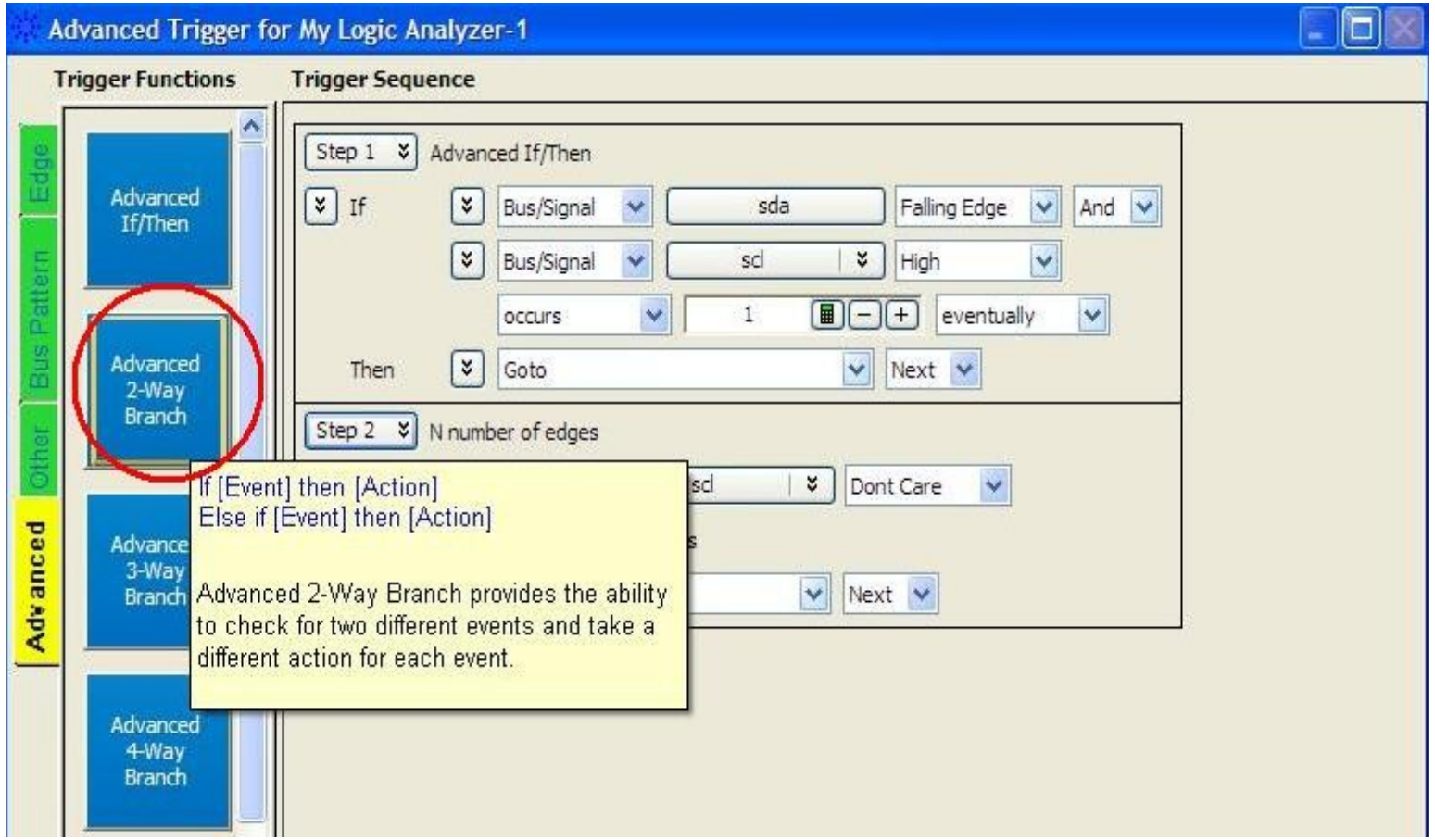
触发举例—I2C总线测量

7、按图设置触发，跳过I2C起始条件后的7个地址位。



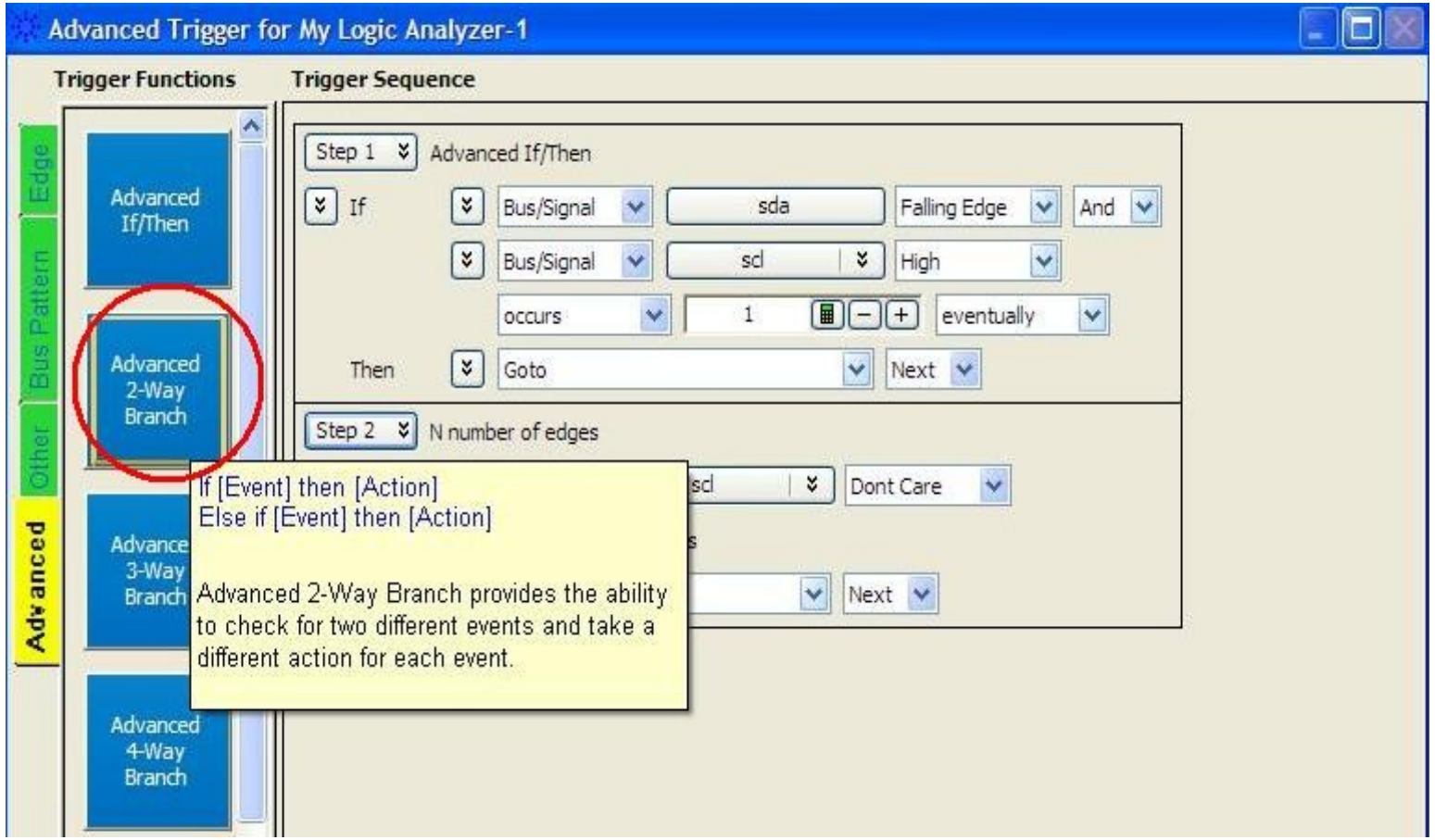
触发举例—I2C总线测量

8、从左边函数中找到“Advanced 2—Way Branch”，拖到第3步的位置，设置一个2分支的触发路径。



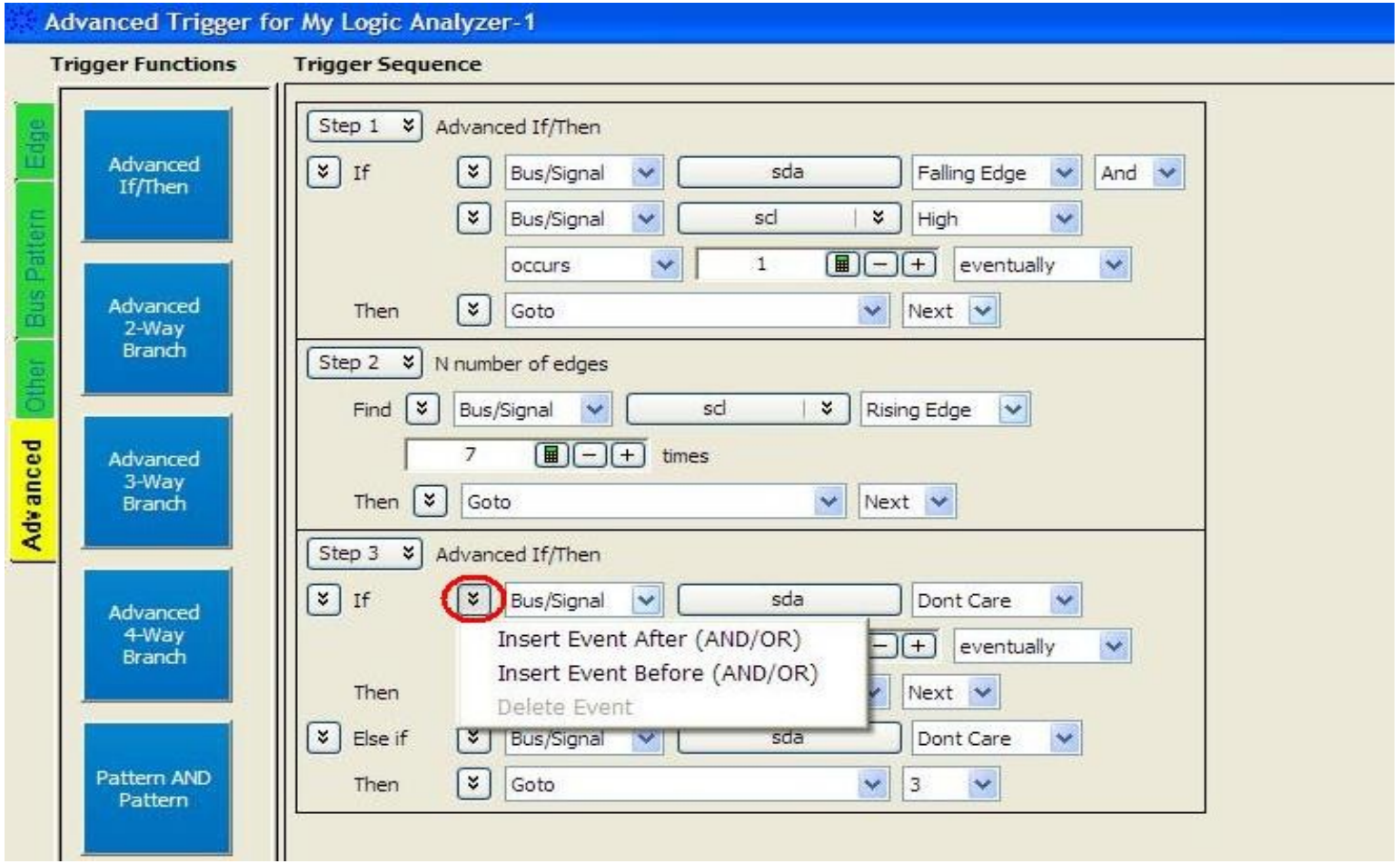
触发举例—I2C总线测量

8、从左边函数中找到“Advanced 2—Way Branch”，拖到第3步的位置，设置一个2分支的触发路径。



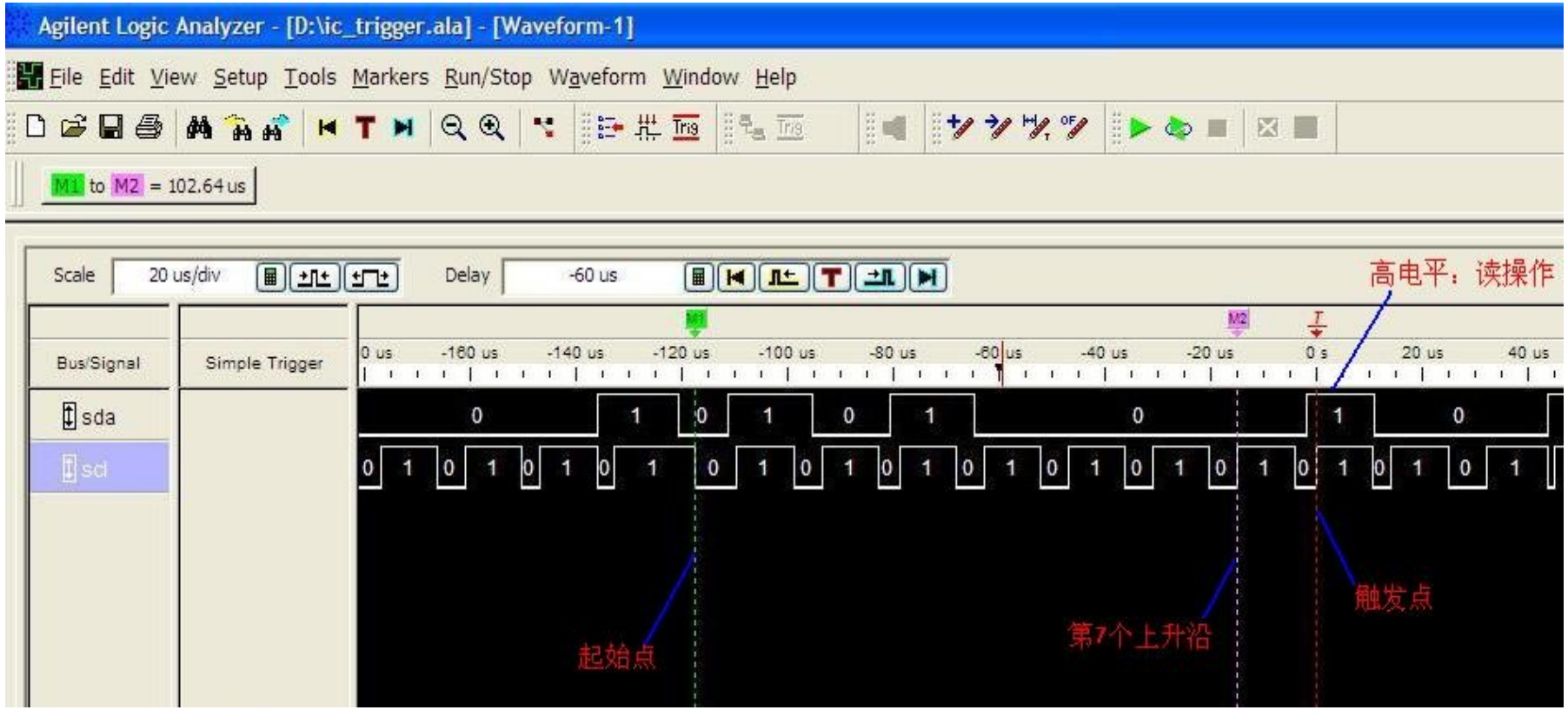
触发举例—I2C总线测量

9、点击”Bus/Signal”前的下拉箭头增加触发条件。



触发举例—I2C总线测量

11、触发设置完成后点“OK”退出，重新运行。从抓到的波 形中判断我们成功抓到了一个I2C的读时序。



逻辑分析仪课程内容

1. 逻辑分析技术

2.逻辑分析仪工作原理

3.逻辑分析仪的触发

4.逻辑分析仪的探头应用

5.逻辑分析仪的测试应用

逻辑分析仪对探头的要求

- Low Signal Loading
- High Connector Density
- Low Clearance
- Ease of Attachment
- Good Reliability

The probe is part of the circuit. The circuit is part of the probe.

逻辑分析仪探头的种类—通用探头

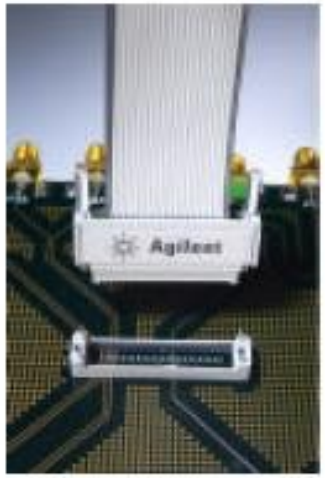
If an Analysis Probe is Not Available, What Should I Use?

Mictor
Up to 600Mb/s
Single-ended only

Samtec
Up to 1.5Gb/s

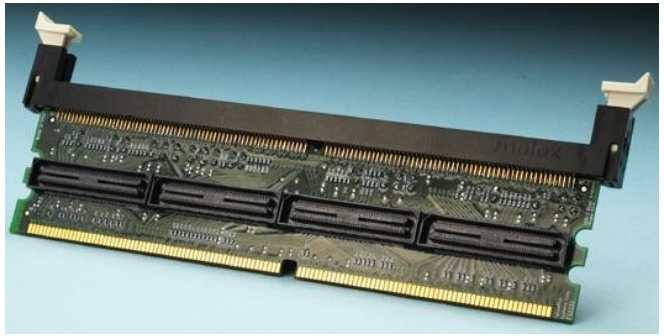
Flying Lead
Up to 1.5Gb/s

Soft-Touch
Up to >2.5Gb/s

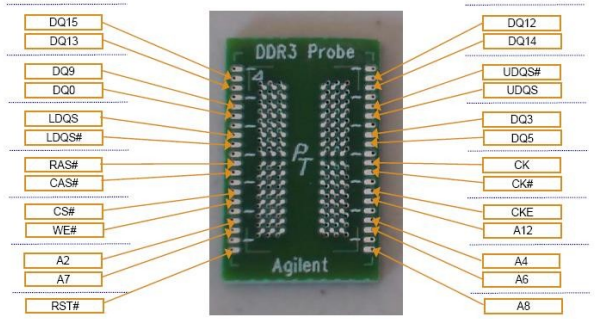


逻辑分析仪探头的种类—分析探头

特定总线分析探头：实现标准总线的探测

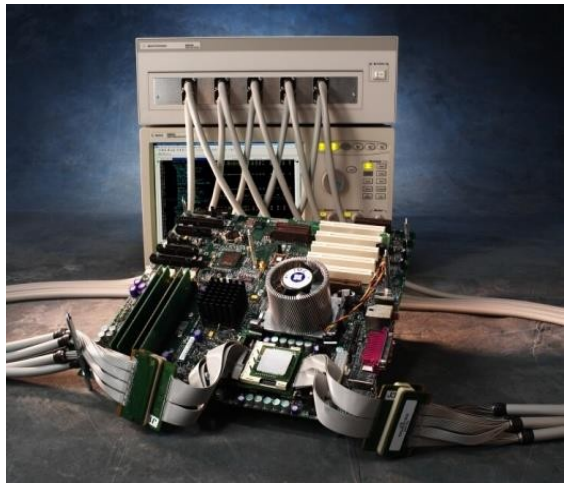


DDR2



DDR3

USB 2.0



FSB

PCI-E

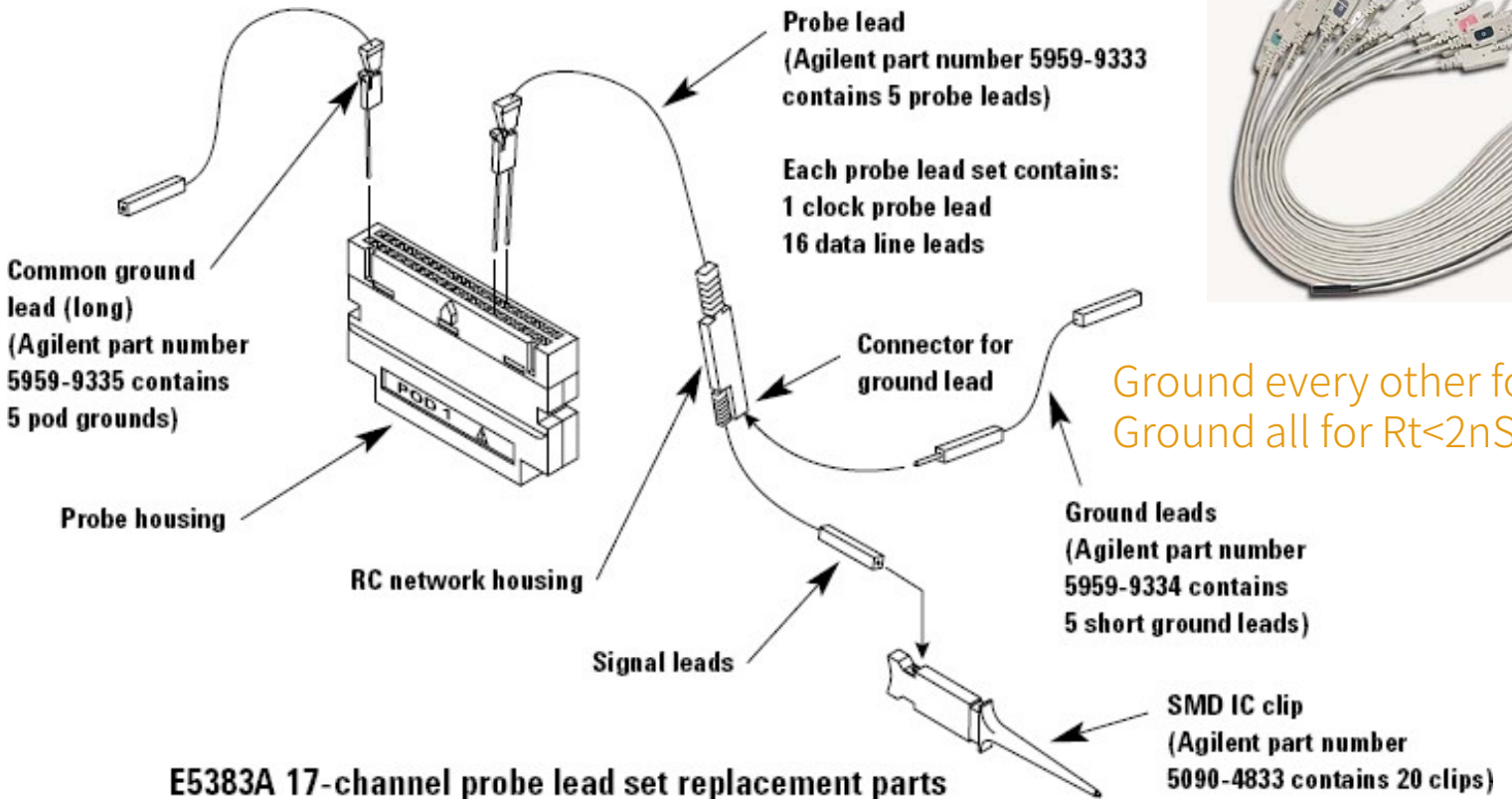
HyperTransport

单端飞线探头—最灵活的探头

17 channels (16 data, 1 clock)

600 mV p-p min. / ±40 volts p-p max.

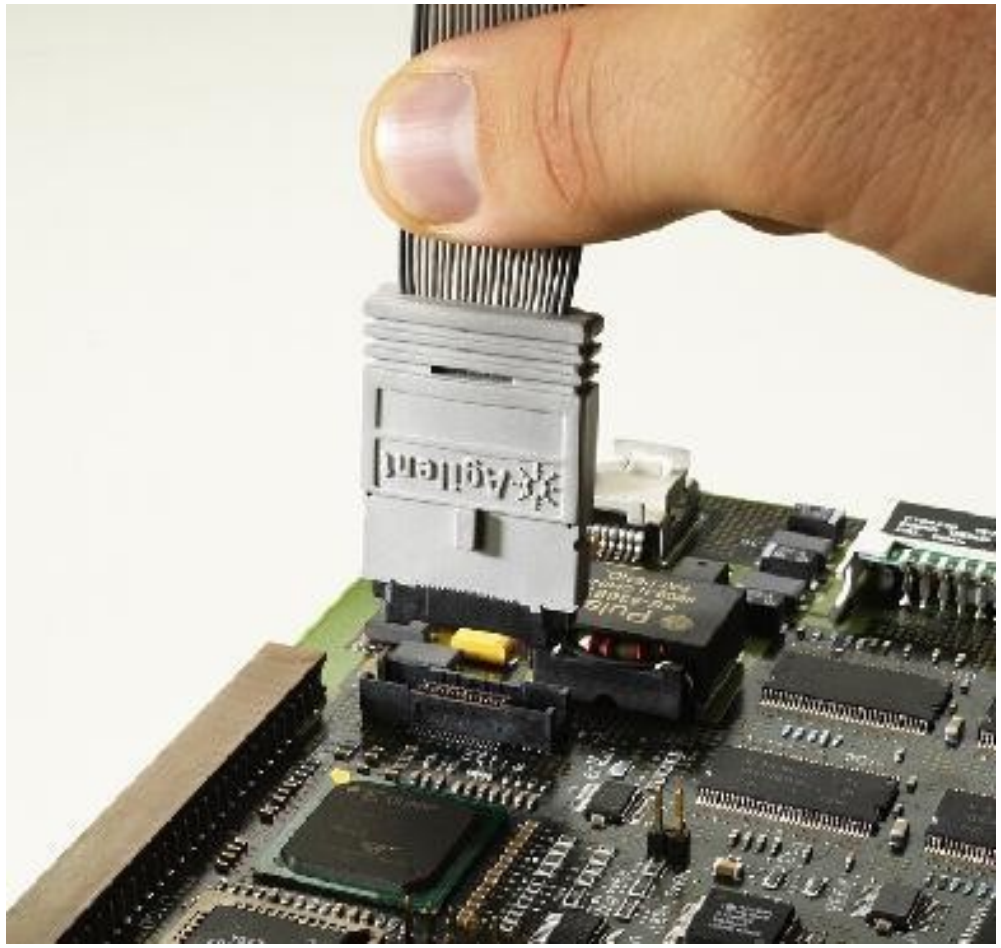
1.5 pF equivalent load capacitance



Ground every other for Rt<5nS
Ground all for Rt<2nS

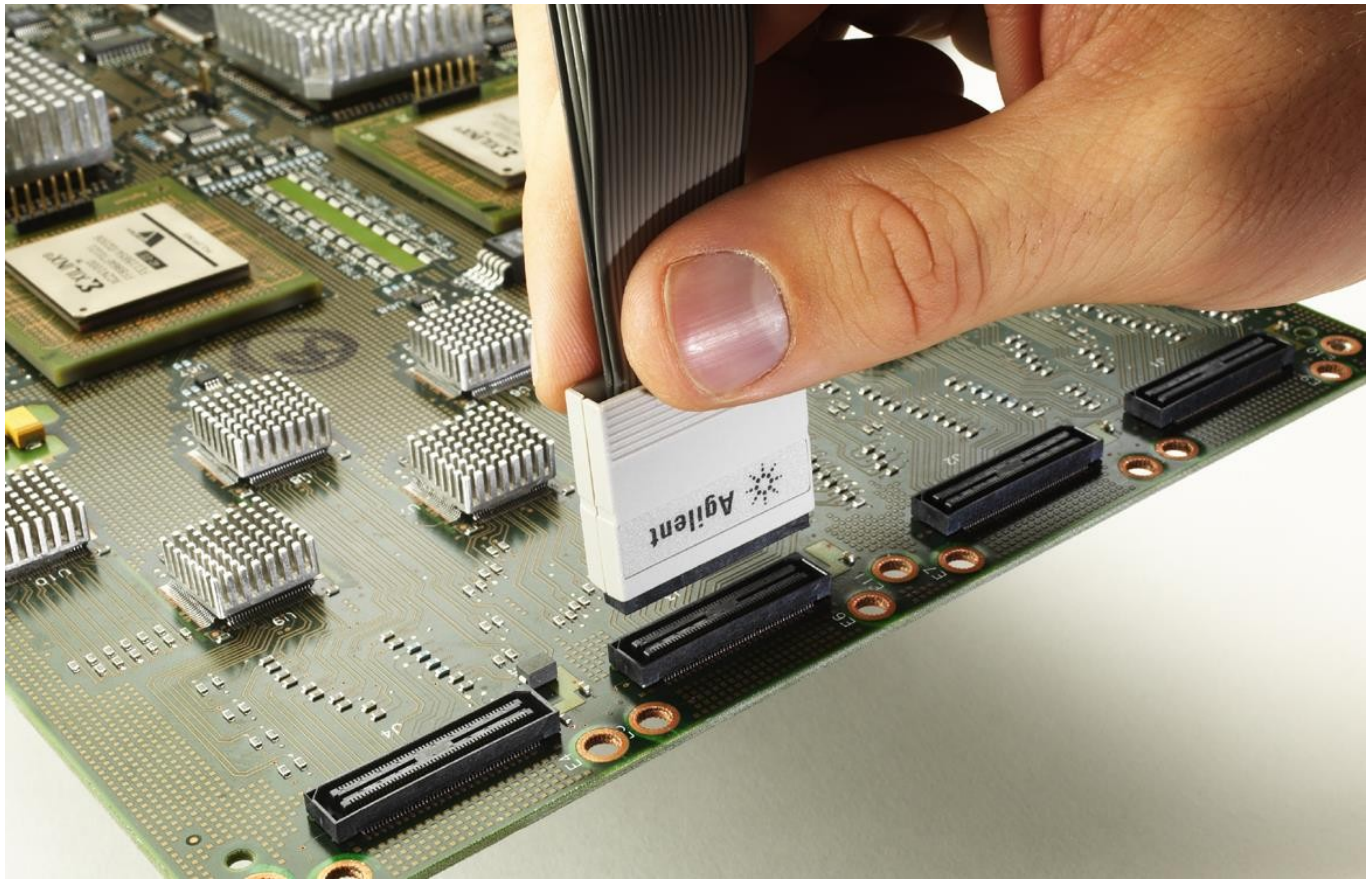
Mictor探头—曾经最流行的高密度探头

- Industry Standard Footprint
- 34 Channels
- 600Mb/s
- 3pF



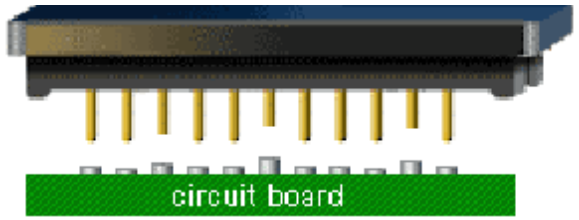
Samtec探头—Agilent的高密度、高速探头

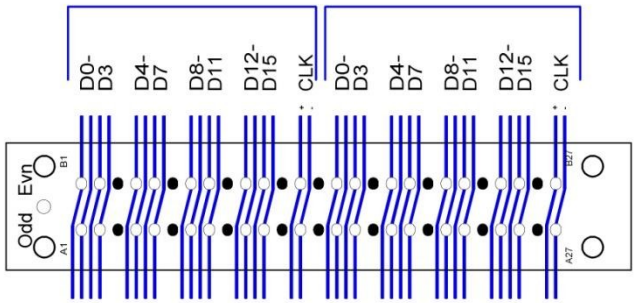
- Keysight Only
- 34 Channels
- 1.5 Gb/s
- 1.5pF



SoftTouch探头—高速信号的唯一探测方案

Reduces Loading to: < 0.7pF
Improves Data rate to: > 2.5Gb
Enables “Flow Through Routing

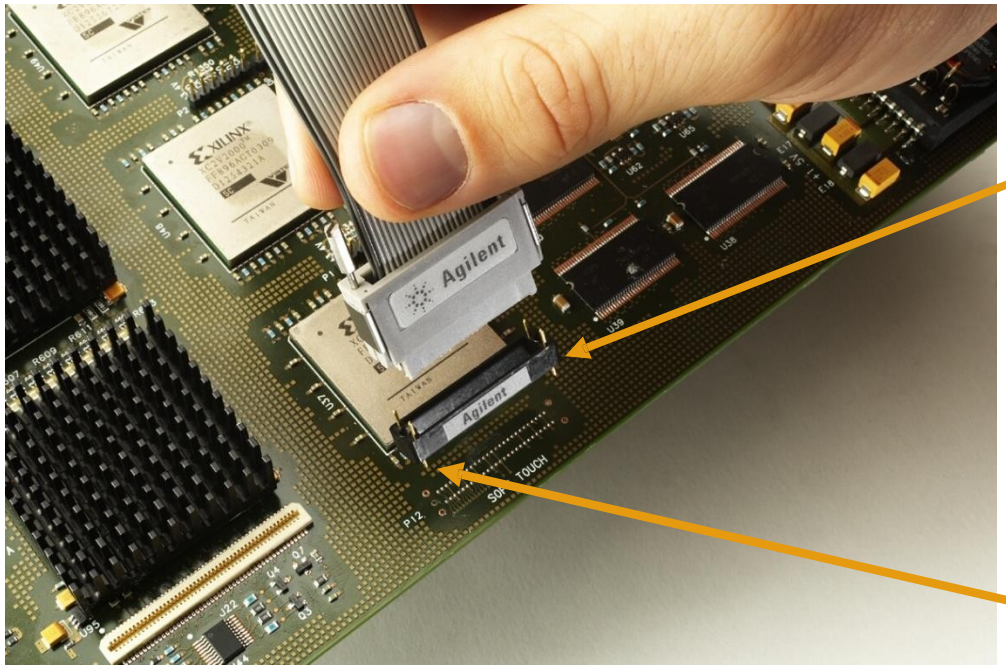


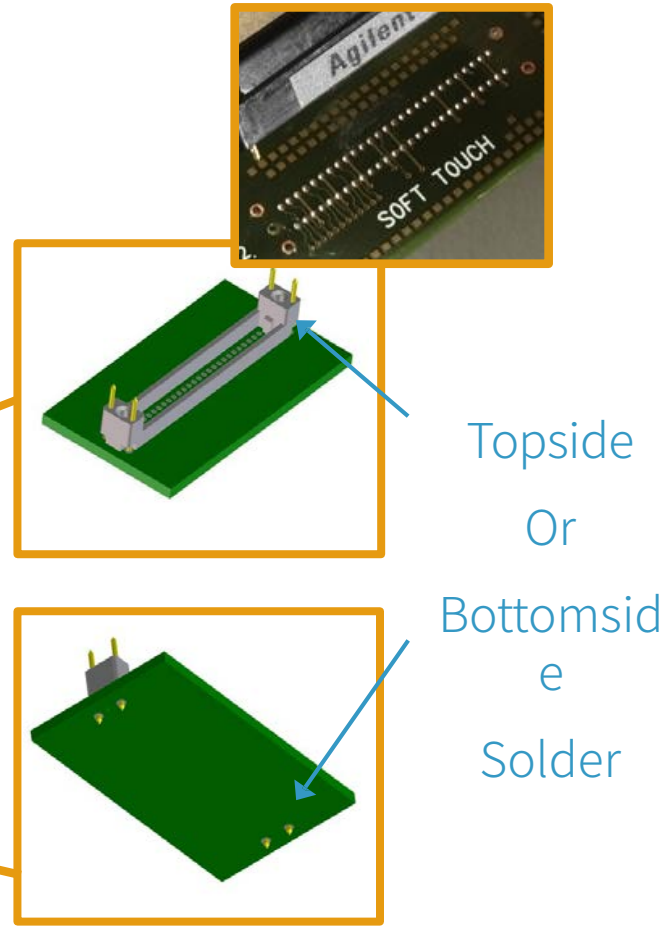


SoftTouch探头的连接方式

Retention Module is Soldered to PCB

*RM is the Mechanical Connection *ONLY*





Topside

Or

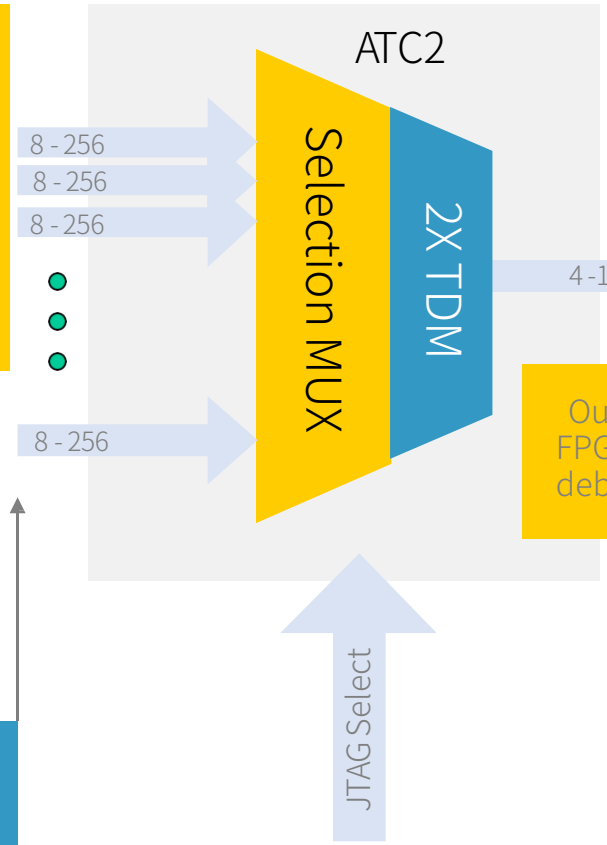
Bottomsid

e

Solder

动态探头的工作原理

- Up to 32 signal banks
- All banks have identical width (4 to 128 signals wide)

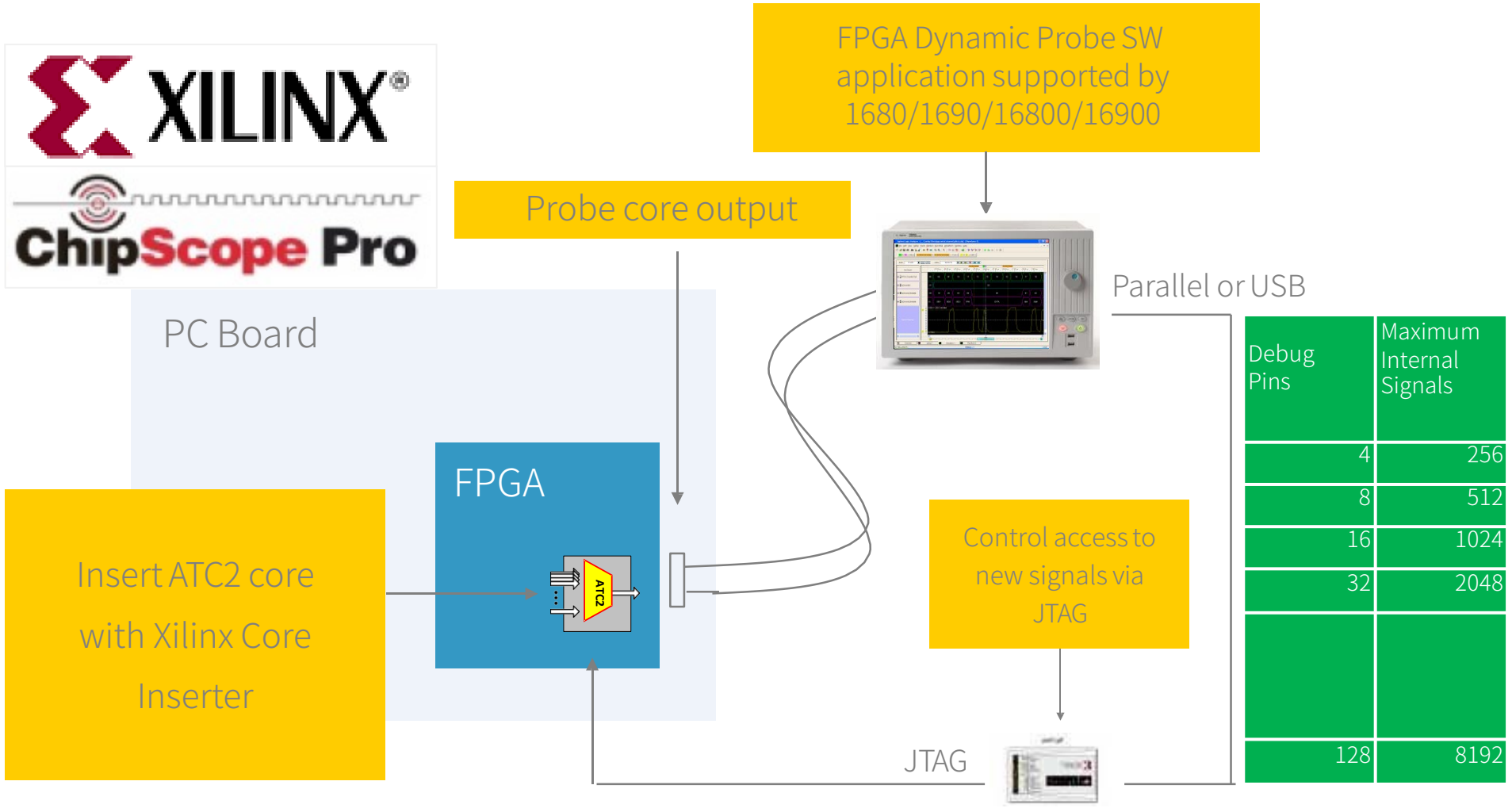


Number of Debug Pins	Maximum Internal Signals
4	256
8	512
16	1024
32	2048
.	.
128	8192

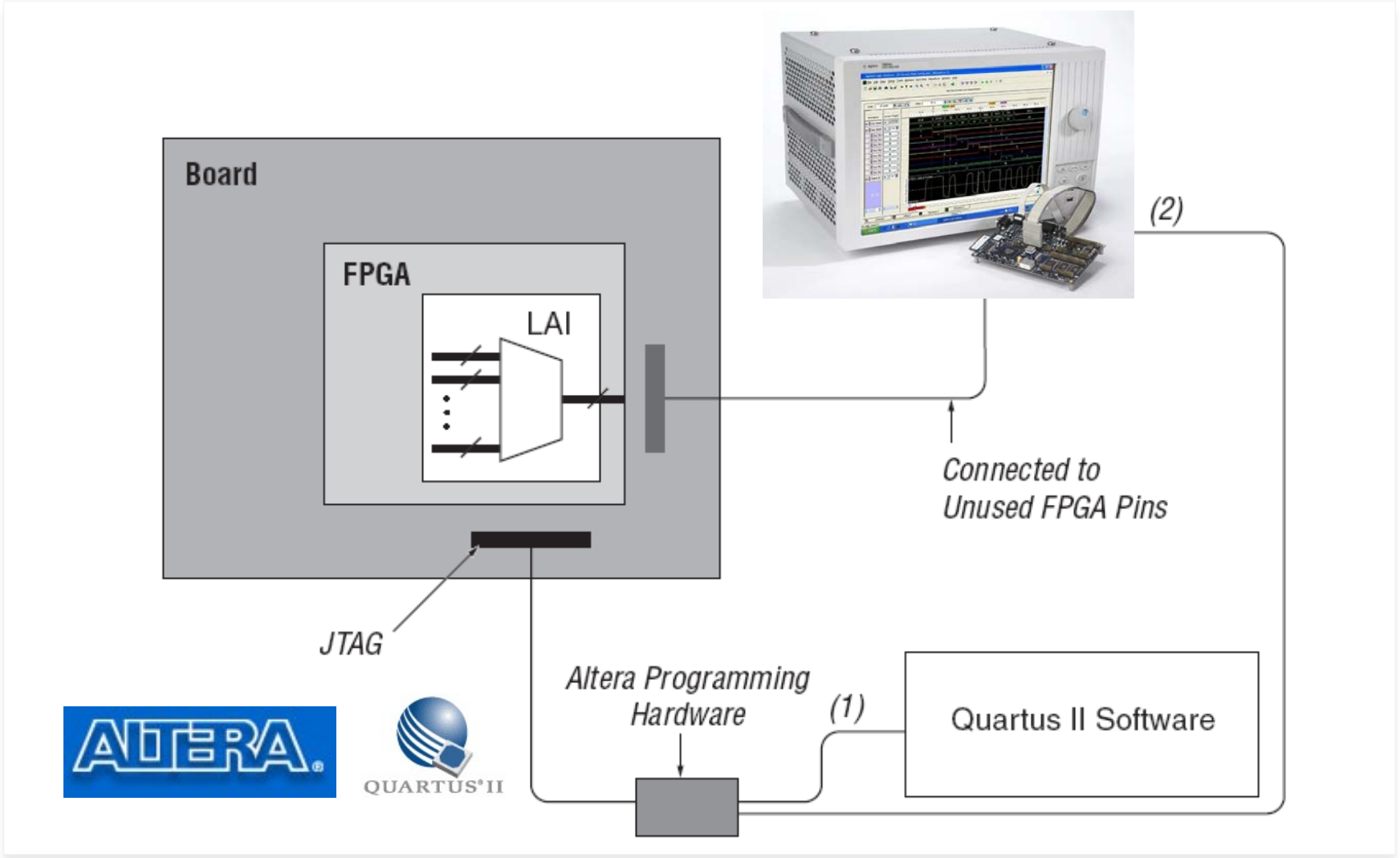
- Pin compression option:
- 2 signals/pin

Change signal bank selection from logic analyzer

动态探头—Xilinx FPGA调试方案



动态探头—Altera FPGA调试方案



逻辑分析仪课程内容

1. 逻辑分析技术

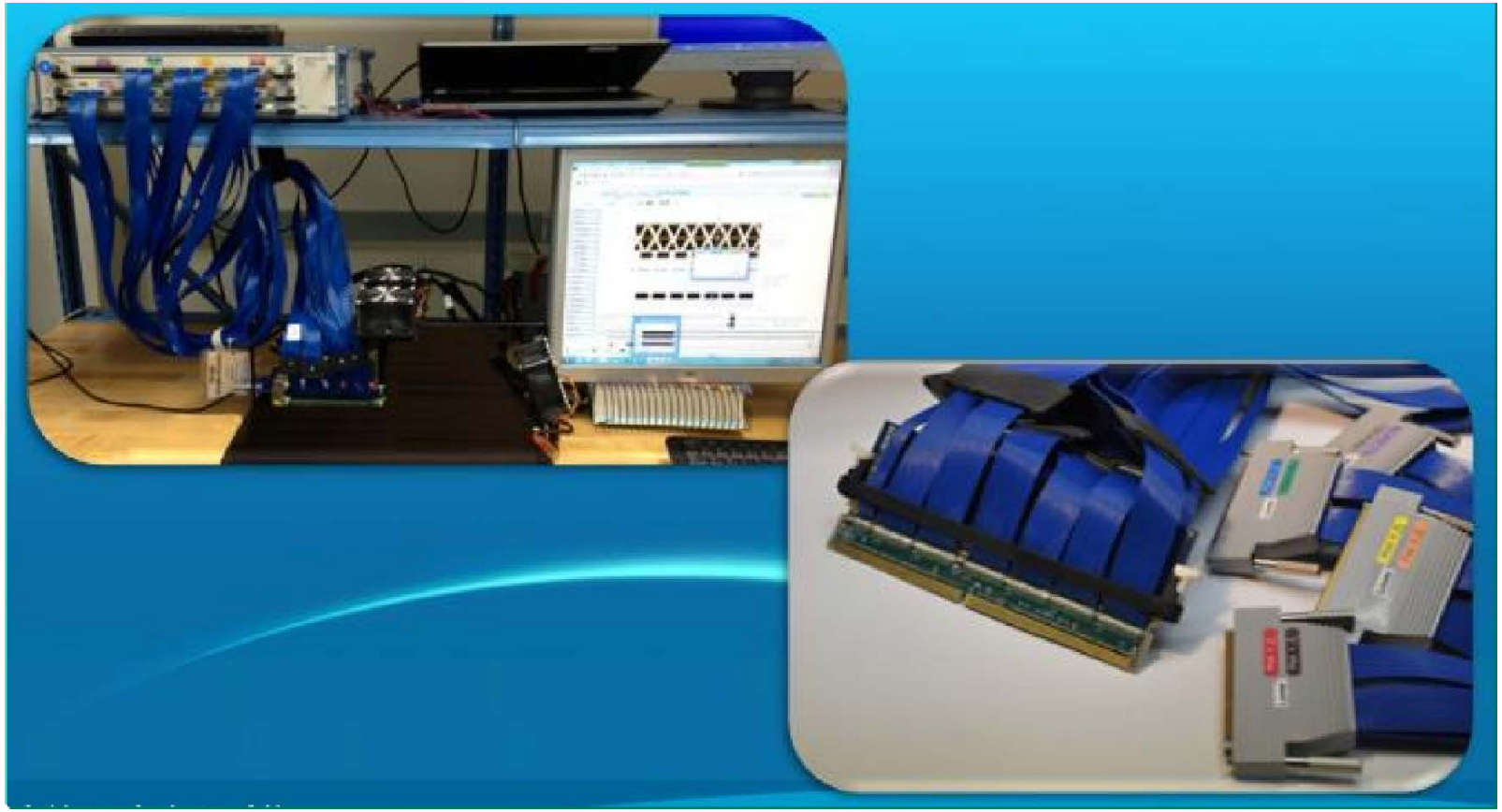
2.逻辑分析仪工作原理

3.逻辑分析仪的触发

4.逻辑分析仪的探头应用

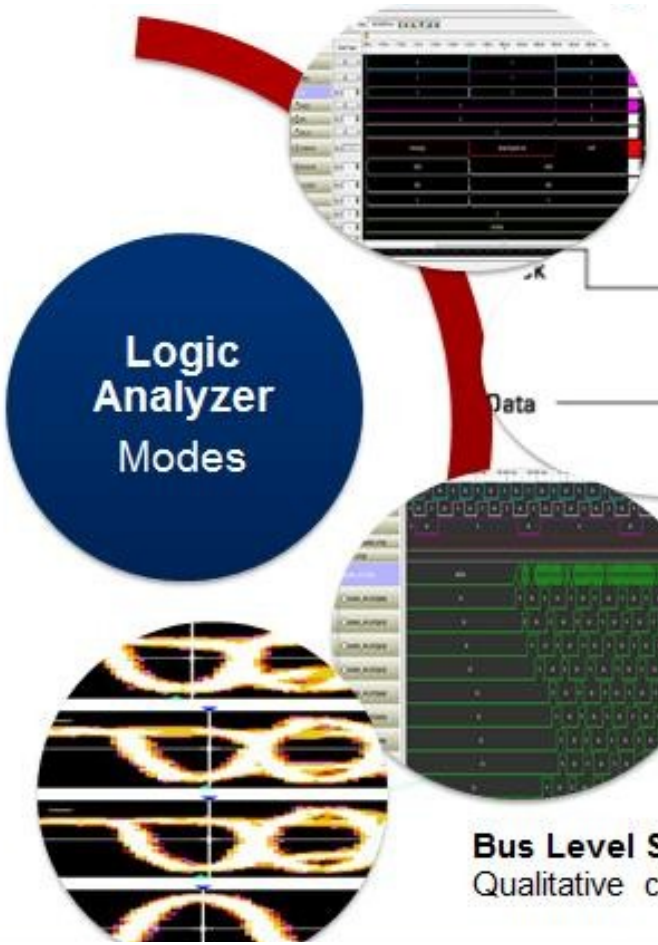
5.逻辑分析仪的测试应用

DDR4 Debug and Protocol Validation Challenges



类脑智能 驱动未来

Benefits of Logic Analysis



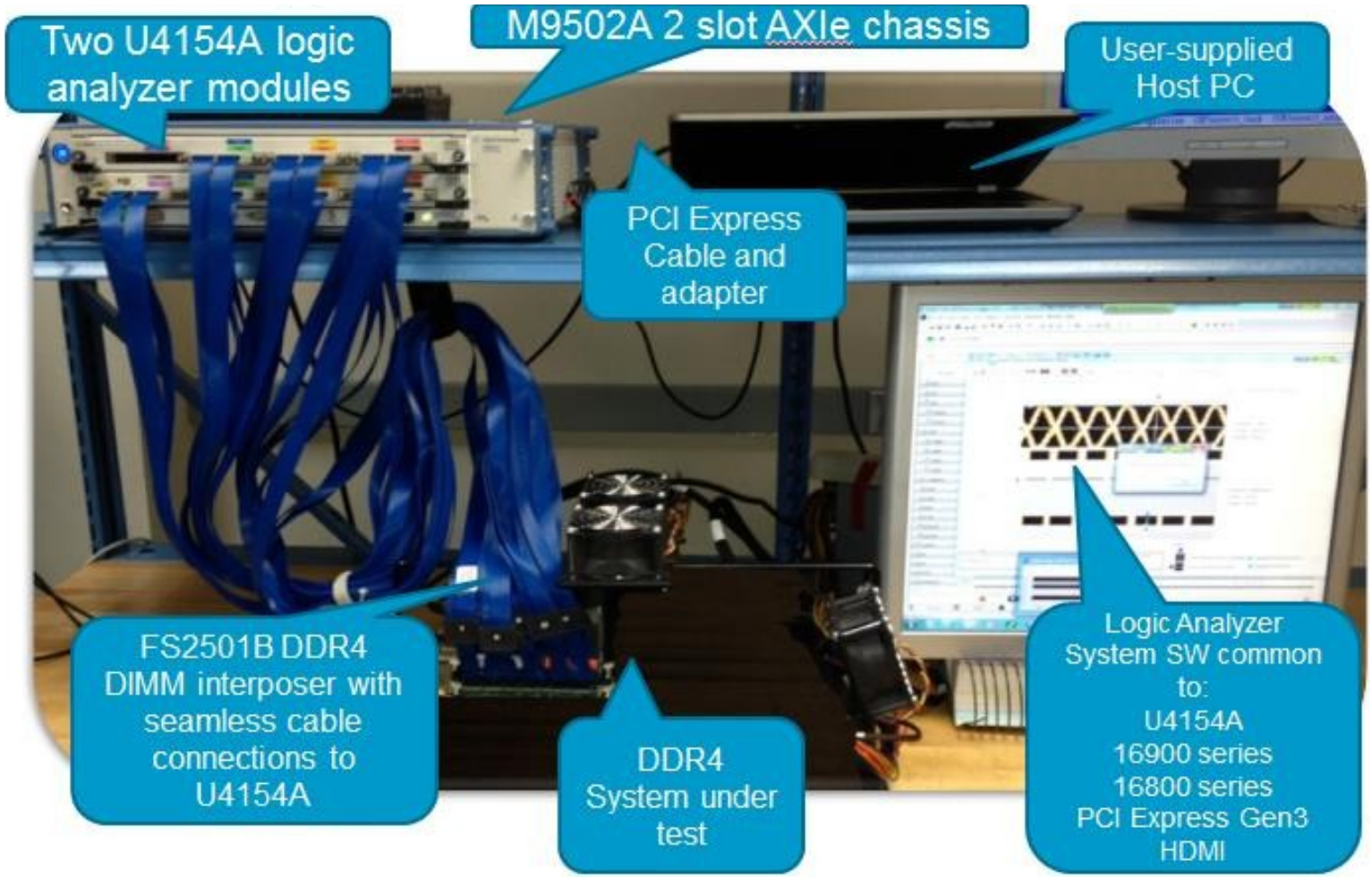
View when events happened.
Timing mode and Transitional Timing Modes
Asynchronous to system under test.

Follow what happened
State Mode
Synchronous to clock from system
Enables most powerful SW tools

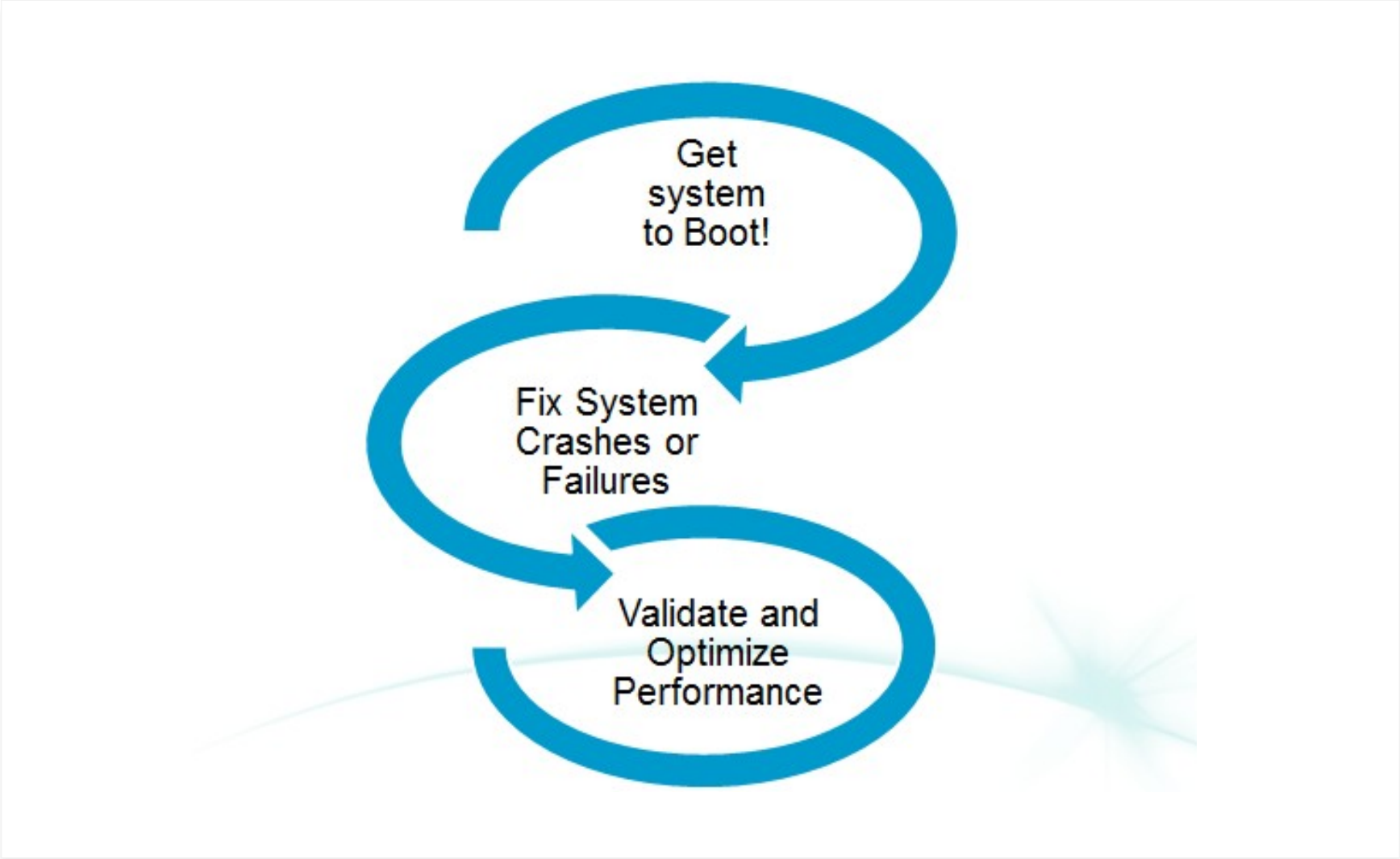
High resolution around trigger event.
Timing Zoom
Simultaneous with State or Timing modes

Bus Level Signal Integrity Insight – Eye Scan
Qualitative comparison of eye diagrams relative to each other

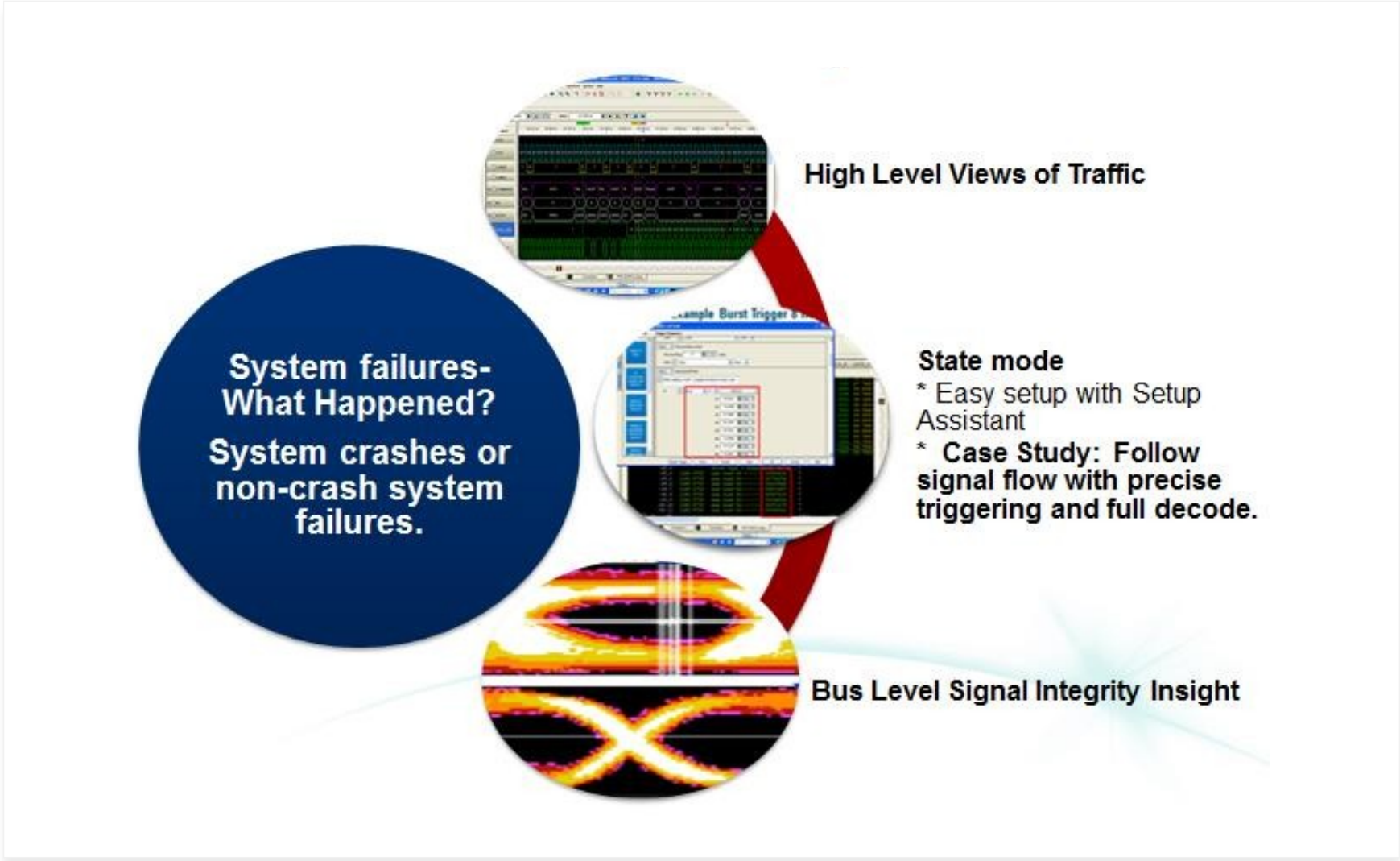
U4154A Typical DDR4 DIMM Configuration



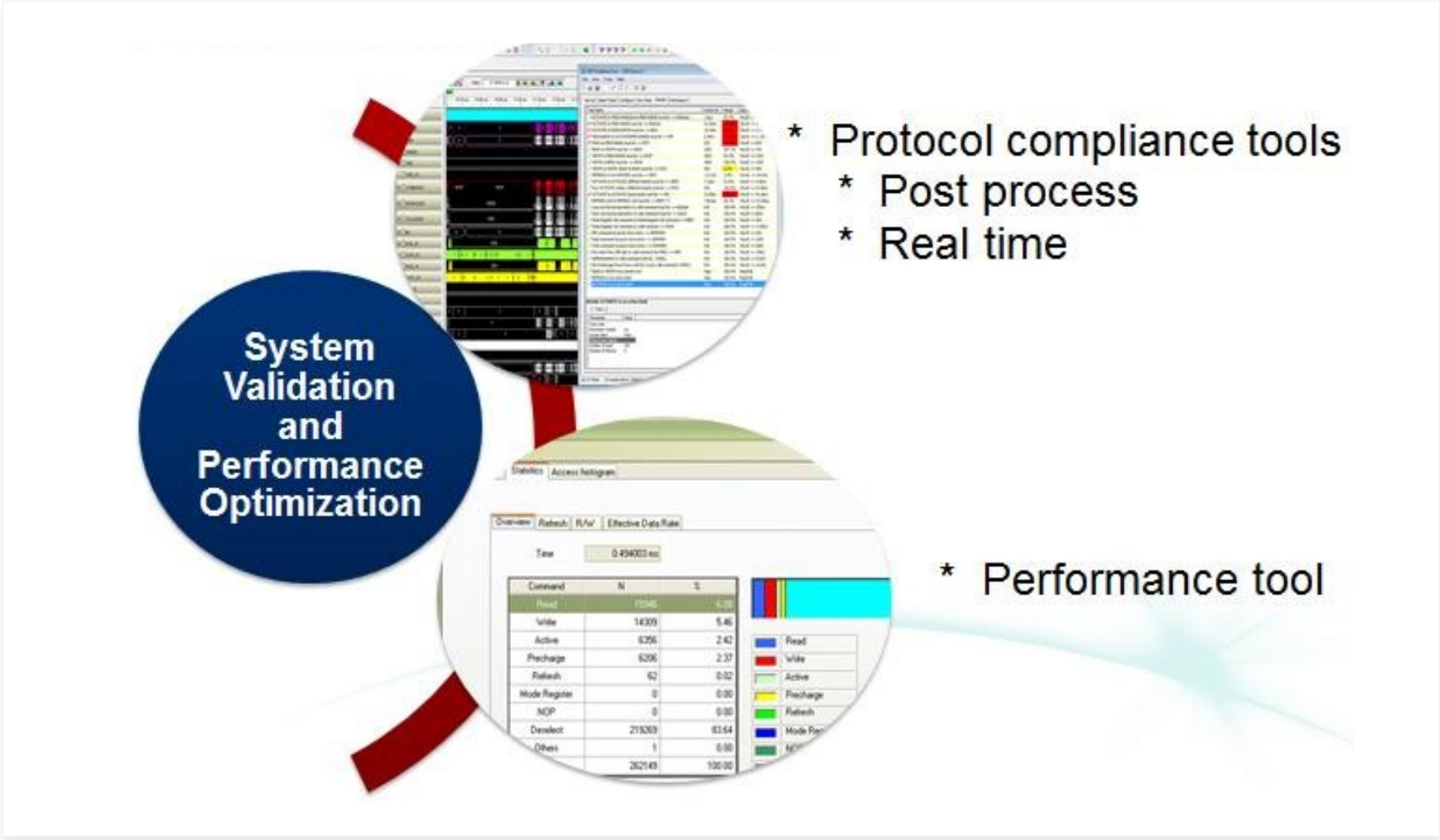
Simplified Debug and Validation



Test Tools and Techniques for System Failures



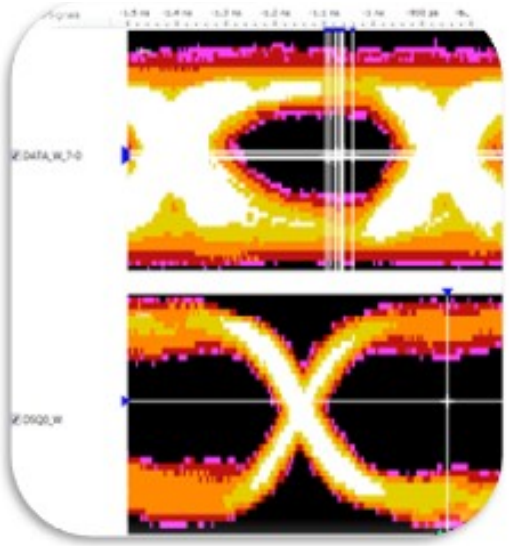
Test Tools and Techniques for System Validation and Optimizing Performance



CS: Following the Signal Flow Next steps…

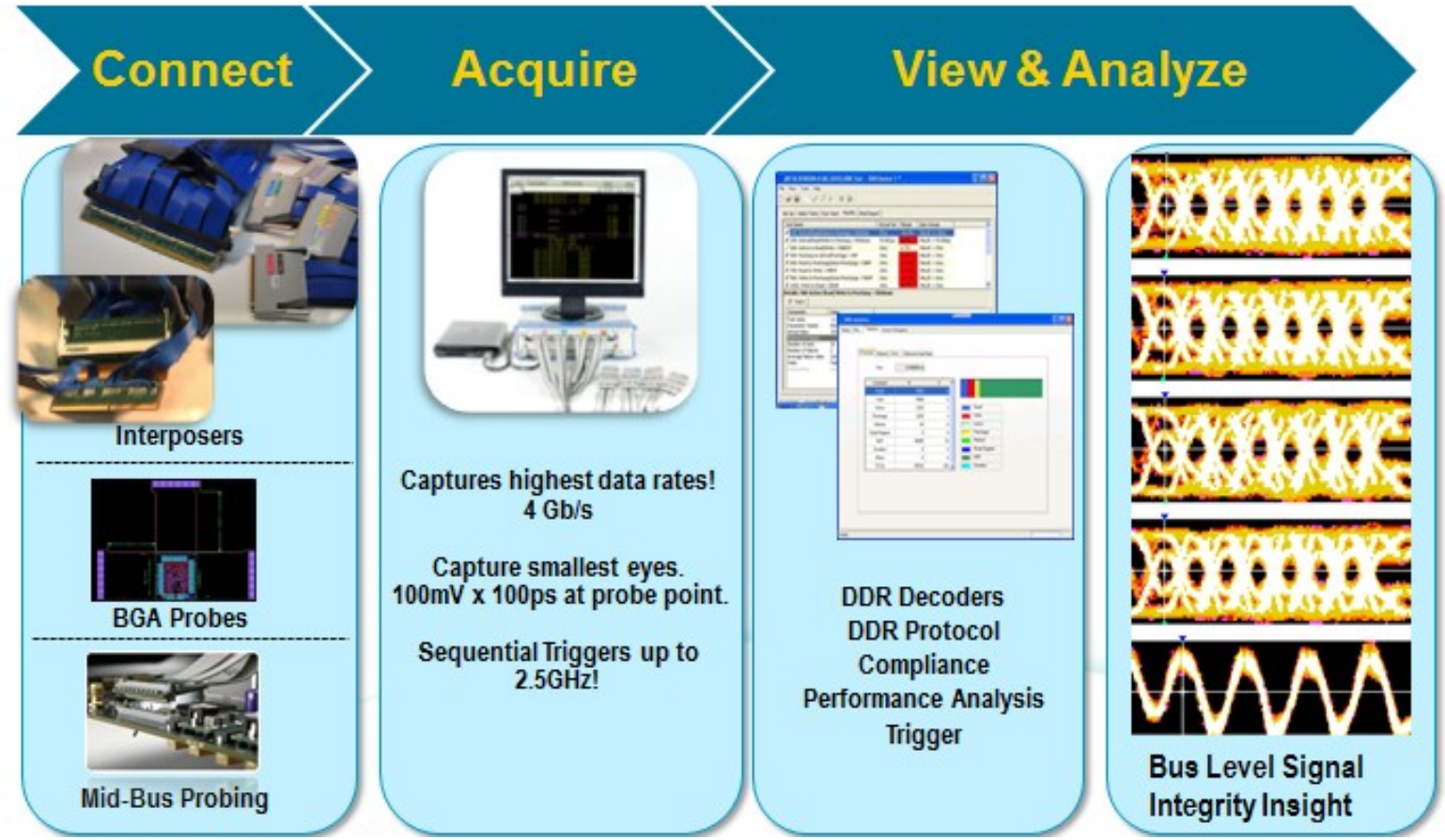
Check Write Eye Scans

- Does DQS to DQ relationship look correct?
  - DQS Write edge approx centered on DQ eye
  - Sytem variable, know your system!
- If an issue is seen:
  - Observe high resolution timing traces Writes
  - Cross trigger scope from LA

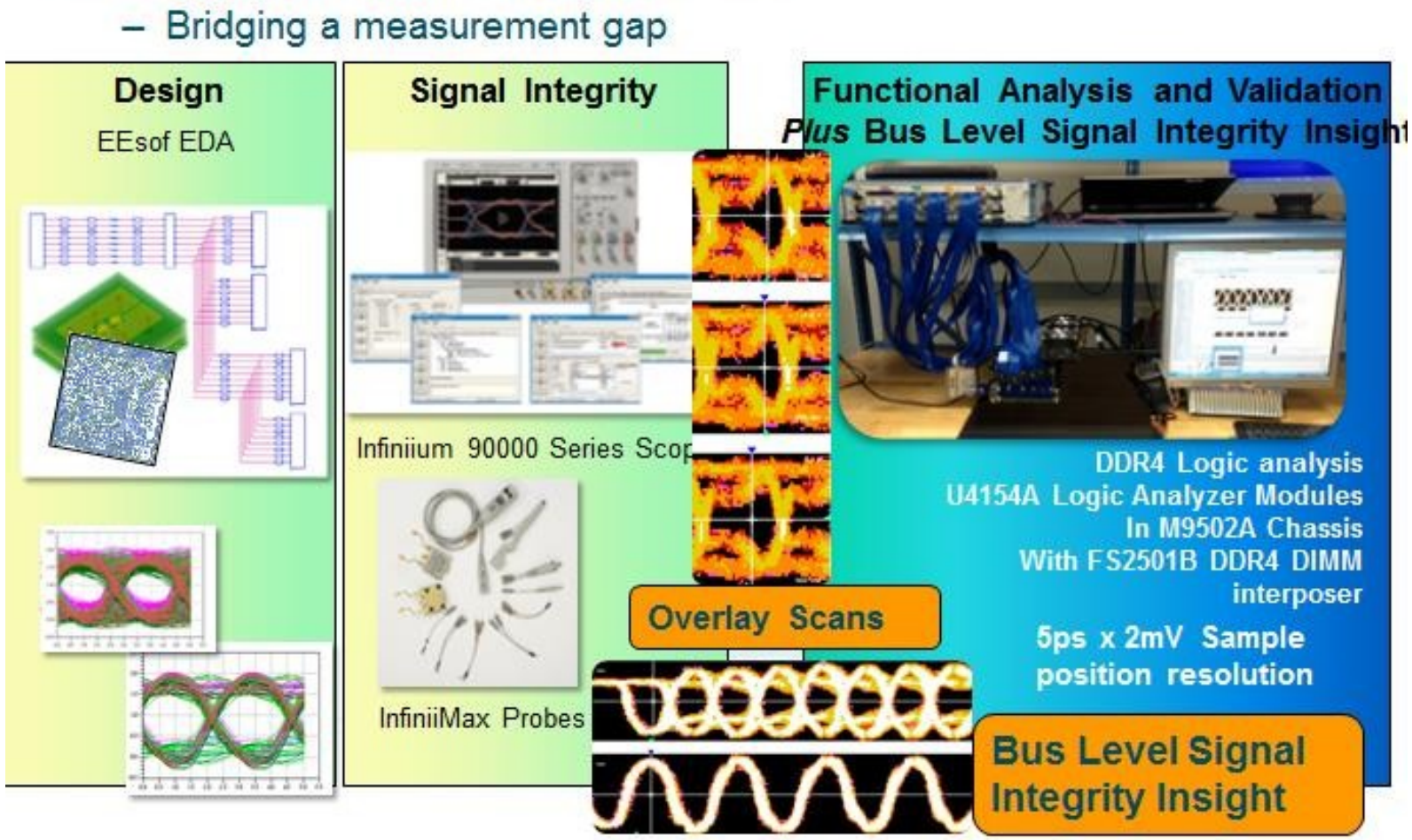


Next: Run Protocol Validation tools ..errors can corrupt Writes to memory.

Logic Analyzer solutions for DDR4



Bus Level Signal Integrity Insight




类脑智能
驱动未来
THANKS
NeuHelium
新氦类脑智能
类脑智能
驱动未来
BY
NeuHelium